Technical Requirements Specification

Technical specification for Design, Manufacturing, Test, Installation and Commissioning of ITER VS3 Power Supply

Technical specification for Design, Manufacturing, Test, Installation and Commissioning of ITER VS3 Power Supply

	Approval Process		
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Change Log			
Technical specification for Design, Manufacturing, Test, Installation and Commissioning of ITER VS3 Power Supply (EFXUVH)			
Version	*Latest Status*	*Issue Date*	*Description of Change*
v1.0	Signed	19 Dec 2025	
v2.0	Revision Required	19 Feb 2026	Major revision introducing new sections, supplementing existing content, and integrating feedback from reviewers.
v2.1	Approved	12 Mar 2026	Minor revision addressing comments from reviewers.

TECHNICAL SPECIFICATION FOR

Design, Manufacturing, Test, Installation and Commissioning of ITER VS3 Power Supply

Technical Specification – VS3 Power Supply (41.V3)

Table of Contents

1 Preamble

This is the Technical Specification for the Task Agreement (TA) covering the turnkey procurement of the VS3 Power Supply System (41.V3).

This technical specification is to be read in conjunction with the General Management Specification for Service and Supply (GM3S) [AD1] that constitutes a full part of the technical requirements.

This version is subject to changes to align with the clarifications issued during the process of Task Agreement tender.

1.1 Order of precedence

Any ambiguity, conflict or inconsistency between the documents comprising this Specification shall be resolved according to the following order of precedence (from higher to lower):

1. VS3-PS Technical Specification (this document)
2. General Management Specification for Service and Supply (GM3S) [AD1]
3. Applicable Codes & Standards (section 4.2)
4. Interface Control Documents and Interface Sheets (listed in section 4.1.1)
5. Applicable Documents (section 4.1.1)

Should any uncertainty arise, the DA is strongly advised to seek clarification from IO.

2 Purpose and Scope

2.1 Background and system overview

2.1.1 ITER

The ITER Organization (IO) is a joint international research and development project of fusion. The seven members of the IO are: the European Union (represented by F4E), Japan, the People's Republic of China, India, the Republic of Korea, the Russian Federation and the USA.

The project aims to demonstrate the scientific and technological feasibility of fusion power for peaceful purpose and to gain necessary data for the design, construction and operation of the first electricity-producing fusion plant. It will also test a number of key technologies, including the heating, control, diagnostic and remote maintenance that will be needed for a full-scale fusion power station.

The ITER site is in the Bouches-du-Rhône department of France. It includes the Headquarters of the IO and a construction worksite. The construction of the facility is on-going. Further information is available on the IO website: www.iter.org.

2.1.2 Coil Power Supply and Distribution

The ITER plant is hierarchically broken down into plant systems, in accordance with the ITER Plant Breakdown Structure (PBS) [RD1]. The VS3 Power Supply in the scope of this Technical Specification belongs to PBS 41 – Coil Power Supply & Distribution.

The Coil Power Supply and Distribution (CPSD) plant system comprises the following major subsystems:

- Pulsed Power Electrical Network (PPEN), stepping down the 400kV grid connection and distributing it to pulsed power loads at 66kV and 22 kV levels
- Reactive Power Compensation and Harmonic Filtering (RPC&HF), reducing the reactive power flow, voltage fluctuations and distortion caused by ITER pulsed power loads
- AC/DC power converters for plasma initiation, current drive, shape and position control, and error field correction, comprising:
    - Ex-Vessel Coil Power Supplies, driving ITER's superconducting TF, CS, PF, and CC magnets with a total installed capacity of 2.2 GVA
    - In-Vessel Coil Power Supplies, driving the 27 ELM coils for ELM, RWM and Error Field control and the VS coils for fast vertical stabilization of the plasma.
- Switching Network Units, Fast Discharge Units, Busbars and Instrumentation & Control

2.1.3   VS3 Power Supply System

Operation of ITER requires fast active control of the plasma's vertical position, which is accomplished through the Vertical Stabilization (VS) coils that reside inside the Vacuum Vessel. The VS coils consist of an upper and lower solenoidal coil, VS3U and VS3L respectively, connected in an anti-series "saddle" arrangement. Both the upper and lower coil are comprised of four individual turns, interconnected by the VS3 Linkboard (41.V3.BB).

The plasma's vertical position is stabilized by a feedback system that typically measures the vertical drift velocity and controls the current in the VS coils to generate a horizontal magnetic field that counteracts the vertical displacement. The VS coils thus exert a downward force when the plasma drifts upwards, and vice versa. The fast response rate needed for vertical stabilization is a strong driver for the power supply requirements and design.
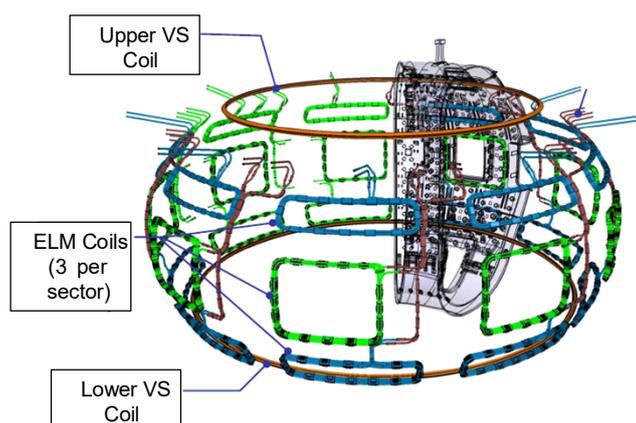
Figure 2-1: Overview of in-vessel coils

The VS3 Power Supply provides the controlled current or controlled voltage in the anti-series connected VS3U and VS3L coils. The power supply comprises two independent power converters, each with a large capacitor bank for storing the energy required to inject in the coil circuit during a VDE pulse, connected to the VS coils in a so-called push-pull configuration.

Technical Specification – VS3 Power Supply (41.V3)
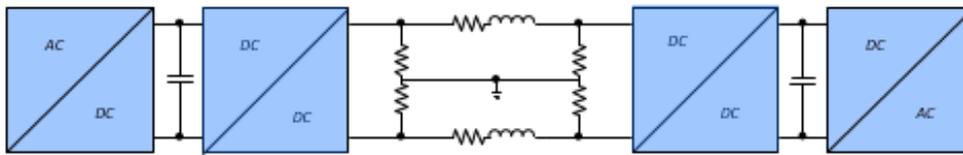
Figure 2-2: VS3 Power Supply comprising two power converters in push-pull configuration

The VS3 Power Supply is required for all operational stages defined in Baseline 2024, i.e. SRO, DT-1 and DT-2 [AD5].

2.1.3.1 *Plant Breakdown Structure*

Within the framework of ITER's Plant Breakdown Structure [RD1], the VS3 Power Supply System is broken down into the Level 3 subsystems listed in Table 2-1.

Table 2-1: VS3 Power Supply nodes in PBS structure

Node	Title	Notes
41.V3.00	Common	Includes Cable Trays, Cables, CCWS components, LV distribution, MV feeders, Switchgear, Supports, etc.
41.V3.CH	Charger	Includes Transformer
41.V3.CP	Capacitor Bank	
41.V3.CR	Crowbar	
41.V3.DL	Dummy Load	
41.V3.IC	Plant System I&C	
41.V3.SA	Mechanical Structures	
41.V3.BB	VS3 IVC Busbars, Supports, Links and Linkboard	Not in scope of this procurement (apart from interface)
41.V3.BE	Extension busbars, supports and links	Not in scope of this procurement (apart from interface)

2.2 Responsibilities

2.2.1 *DA's responsibilities*

The DA is responsible for the preliminary design, final design, manufacturing, factory tests, inspections, delivery, installation, assembly, integration, site acceptance tests, integrated commissioning on dummy load and support to the integrated commissioning on the VS coils, associated to the scope of supply under this Technical Specification.

The DA is responsible for the development of a design that meets all requirements set out in this Technical Specification. The design shall be performed in accordance with applicable design codes, QA requirements and standards listed in this Technical Specification. Any deviations and

Technical Specification – VS3 Power Supply (41.V3)

non-conformances shall be done in accordance with requirements of Procedure for the management of Deviation Request [AD8] and Procedure for Management of Nonconformities [AD9].

2.2.2 IO's responsibilities

IO is responsible for providing the functional technical specifications, including the requirements related to interfaces and integration, such as on space limitations, access restrictions, services available, etc.

IO takes responsibility for the management of interfaces with other ITER plant systems, such as CCWS, PPEN, SSEN, CTS, CODAC, CIS, PCS, etc., with the technical input from the DA.

IO also takes responsibility for the integrated circuit tests with the VS coils; see the definitions in section 15.1.1.

IO provides the following items and services in relation to this TA:

- Area for storage and pre-assembly of equipment and fabricated elements at ITER premises;
- Data, items and services defined under IO responsibility in the ICD and corresponding IS;
- Guidance to the DA on the execution of site related physical activities at the ITER site, in compliance with applicable HSE norms.

The responsibilities of DA and IO in relation to the physical interfaces is covered in detail by Section 5.2 - Physical Connection Points on Boundaries of Supply and Installation.

2.3 Work Schedule

In accordance with the latest ITER Project Schedule issued in the framework of Baseline 2024, IO has developed an associated high-level schedule requirement for this TA. The DA is responsible to develop and control the detailed schedule.
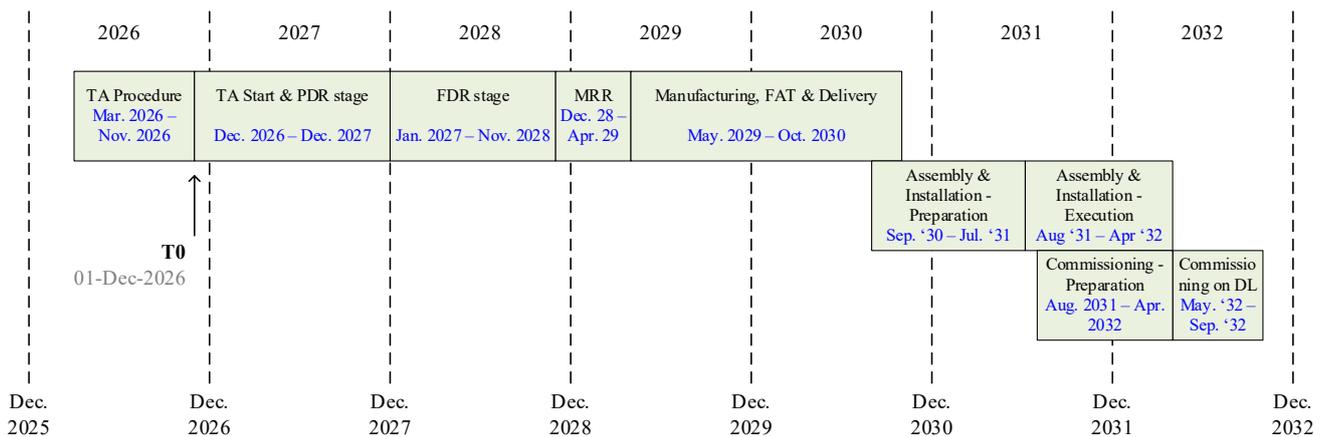
Figure 2-3: high-level work schedule for VS3-PS TA

A more detailed milestone schedule is included in section 20.1.

3 Acronyms & Definitions

3.1 Acronyms

Acronyms	Description
CCS	CODAC Core System
CDR	Conceptual Design Review
CIN	Central Interlock Network
CIS	Central Interlock System
CNP	Central I&C Network Panel – network interconnection point
CODAC	COntrol, Data Access and Communication
COTS	Commercial Off The Shelf
cRIO	compactRIO (National Instruments I&C platform)
CRR	Construction Readiness Review
CS	Central Solenoid
CTS	Cable Tray System
DA	Domestic Agency
DAN	Data Archiving Network
DPP	Document Production Plan
DRR	Delivery Readiness Review
EMI	Electromagnetic Interference
EPICS	Experimental Physics and Industrial Control System
ESCB	Energy Storage Capacitor Bank
EWP	Engineering Work Package
FDR	Final Design Review
FMECA	Failure Mode, Effects, and Criticality Analysis
FRS	Floor Response Spectra
FSR	Full-Scale Range
GM3S	General Management Specification for Service and Supply
HIRA	Hazard Identification and Risk Assessment
HMI	Human Machine Interface
HPSR	High Potential Severity Rate
I&C	Instrumentation and Control
IDP	Input Data Package
IDS	Interface Data Sheet
IFP	Interface Point
IO	ITER Organization
IS	Interface Sheet
IVC	In-Vessel Coils
LDSR	Lost Days Severity Rate
LTIR	Lost Time Injury Rate
LV	Low Voltage
MKIS	Mechanical Key Interlock System

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MPP	Metallized Polypropylene
MQP	Management and Quality Program
MRR	Manufacturing Readiness Review
MV	Medium Voltage
NC	Non-Conformity
NDT	Non-Destructive Test
NTP	Network Time Protocol
OPC	Open Platform Communications
OPC UA	OPC Unified Architecture
PBS	Plant Breakdown Structure
PDA	Post Drill Anchor
PDR	Preliminary Design Review
PDS	Post Drill System
PF	Poloidal Field
PIS	Plant Interlock System
PLC	Programmable Logic Controller
PON	Plant Operation Network
PPEN	Pulsed Power Electrical Network
PR	Project Requirement
PS	Power Supply
PTPv2	Precision Time Protocol
RT	Real Time
SDN	Synchronous Databus Network
SLD	Single Line Diagram
SSC	System, Structure and Component
SSAT	Sector Sub-Assembly Tool
SSEN	Steady State Electrical Network
TA RO	Task Agreement Responsible Officer
TCN	Time Communication Network
TF	Toroidal Field
TGCS	Tokamak Global Coordinate System
TSN	Time Sensitive Networking
UPS	Uninterruptible Power Supply
VDE	Vertical Displacement Event
VS3	Vertical Stabilization 3

For a complete list of ITER abbreviations refer to: ITER_D_2MU6W5 - ITER Abbreviations

3.2 Definitions

Task Agreement Responsible Officer (TA RO)

Refers to the IO staff member who is assigned the responsibility of a Task Agreement on IO side.

Long-Lead Item

Refers to components or raw materials for which the lead time does not allow meeting the contractual milestone dates if the design and manufacturing phases and the associated gate reviews are executed as per the applicable procedures.

Power Converter

Refers to the complete set of components that implement the function of converting AC power into DC power (and vice versa) with a controlled DC voltage/current provided to the output circuit. It comprises the following main components:

- AC Disconnector Switch & Earth Switch
- Step-down Transformer
- Rectifier
- DC Link with DC Disconnector Switch & Earth Switch
- Energy Storage Capacitor Bank
- Inverter
- Local instrumentation and control system
- Auxiliary components (cooling water, mechanical structures, supports, etc.)

Protection Important Activity (PIA)

Activity important for protecting the interests mentioned under Article L. 593-1 of the Environmental Code (public safety, health and sanitation, the protection of nature and of the environment), *i.e. activity that falls under the technical or organizational provisions mentioned under the second paragraph of Article L. 593-1 of the Environmental Code or that is liable to affect them;"*

Protection Important Component (PIC)

A component which is important for protecting the interests mentioned under Article L.593-1 of the Environmental Code (public safety, health and sanitation, the protection of nature and of the environment), *i.e. structure, equipment, system (programmed or not), material, component or software that is present in the basic nuclear installation or that is under the responsibility of the operator and that implements a function required for the demonstration mentioned under the second paragraph of Article L. 593-1 of the Environmental Code [i.e. the safety demonstration] or that ensures that this function is implemented."*

VS3 Power Supply (VS3-PS)

The VS3 Power Supply includes the two power converters, the crowbars, the I&C system, the main steel structure, and all other auxiliary systems. Within the context of this Technical Specification, the Extension Busbars (41.V3.BE) and IVC Busbars (41.V3.BB) are not considered part of the VS3 Power Supply – apart from forming an interface with said power supply.

4 Applicable Documents & Code and Standards

4.1 Applicable Documents and Reference Documents

Applicable Documents contain additional requirements and must be considered as integral part of this Technical Specification. Reference Documents are listed for information and illustration purposes only.

The use of any document as a design input that is not listed in this section or not formally provided by IO shall be subject to prior approval by IO.

It is the responsibility of the DA to identify and request for any documents that have not been transmitted by IO, including the below list of reference documents. In case of conflicting information, it is the responsibility of the DA to seek clarification from IO.

Upon notification of any revision of the applicable document transmitted officially to the DA, the DA shall advise within 4 weeks of any impact on the execution of the TA. Without response after this period, no impact will be considered. However, any impact discovered beyond this period will be handled via Procedure for the management of Deviation Request [AD8].

4.1.1 Applicable Documents (AD)

Ref.	Title	UID	Version
[AD1]	General Management Specification for Service and Supply (GM3S)	ITER_D_82MXQK	1.4
[AD2]	General Management Specification for Executing Entities at the ITER Site	ITER_D_YX55YY	2.3
[AD3]	Project Requirements (PR)	ITER_D_27ZRW8	7.1
[AD4]	SRD-41 (Coil Power Supply and Distribution)	ITER_D_28B6XQ	6.0
[AD5]	Staged Approach Configuration - PBS Level 3	ITER_D_SNE6G8	4.1
[AD6]	ITER Quality Assurance Program (QAP)	ITER_D_22K4QX	8.5
[AD7]	Quality Requirements for IO Performers	ITER_D_22MFG4	6.3
[AD8]	Procedure for the management of Deviation Request	ITER_D_2LZJHB	9.1
[AD9]	MQP L2 Procedure for Management of Nonconformities	ITER_D_22F53X	10.3
[AD10]	ITER RAMI Analysis Programme	ITER_D_28WBXD	4.6
[AD11]	Working Instruction for Reliability, Availability, Maintainability and Inspectability (RAMI) Analysis	ITER_D_ C8U8V8	1.2
[AD12]	EDH Part 1: Introduction	ITER_D_2F7HD2	1.4
[AD13]	EDH Part 2: Terminology and Acronyms	ITER_D_2E8QVA	1.5
[AD14]	EDH Part 3: Codes and Standards	ITER_D_2E8DLM	1.3
[AD15]	EDH Part 4: Electromagnetic Compatibility (EMC)	ITER_D_4B523E	3.0
[AD16]	EDH Part 5: Earthing and lightning protection	ITER_D_4B7ZDG	3.0
[AD17]	EDH Guide A: Electrical Installations for SSEN Client Systems	ITER_D_2EB9VT	2.7
[AD18]	EDH Guide C: Electrical Installations for EPS Client Systems	ITER_D_2F6BBN	2.5

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[AD19]	IO cabling rules	ITER_D_335VF9	3.3
[AD20]	IO cable catalogue	ITER_D_355QX2	6.13
[AD21]	Design Review procedure	ITER_D_2832CF	7.0
[AD22]	Design Development Procedure	ITER_D_U34DDZ	2.1
[AD23]	ITER System Design Process (SDP) Working Instruction	ITER_D_4CK4MT	4.1
[AD24]	MQP L3 Expected content of System Design deliverables	ITER_D_43S7GL	2.2
[AD25]	MQP L3 Working Instruction for Manufacturing Readiness Review	ITER_D_44SZYP	5.1
[AD26]	Working Instruction for the Delivery Readiness Review (DRR)	ITER_D_X3NEGB	3.0
[AD27]	Working Instruction for Construction Readiness Review (CRR)	ITER_D_QXW4KQ	3.2
[AD28]	Working Instruction for Operations Readiness Review (ORR)	ITER_D_55E54L	1.1
[AD29]	Work Instruction for Producing of the Manufacturing and Inspection Plan	ITER_D_UKQG8M	1.6
[AD30]	Procedure for Identification and Controls of Items	ITER_D_U344WG	2.2
[AD31]	ITER Numbering System for Components and Parts	ITER_D_28QDBS	5.1
[AD32]	Procedure for Transportation of Components to ITER Site	ITER_D_RY5C6Q	3.1
[AD33]	Design Interface Control Procedure	ITER_D_28VNJG	5.3
[AD34]	Working Instruction for Interface Management	ITER_D_3L775F	2.0
[AD35]	Quality Classification Determination	ITER_D_24VQES	6.0
[AD36]	MQP L3 Working Instruction for the Qualification of ITER safety codes	ITER_D_258LKL	3.1
[AD37]	Sign-Off Authority (SOA) for Project Documents	ITER_D_2EXFXU	9.1
[AD38]	VS3-PS Load Specification for B13	ITER_D_DF8LDF	2.4
[AD39]	Load Specifications (LS)	ITER_D_222QGL	6.3
[AD40]	Instructions for EM Analyses	ITER_D_TSZ9KQ	3.3
[AD41]	Procedure for Analyses and Calculations	ITER_D_22MAL7	6.8
[AD42]	Software Qualification Policy	ITER_D_KTU8HH	2.0
[AD43]	ITER Fire Safety Approach	ITER_D_25SDBD	3.1
[AD44]	ITER Seismic Nuclear Safety Approach	ITER_D_2DRVPE	1.6
[AD45]	ITER Cabling Handbook	ITER_D_4NS2EM	1.0
[AD46]	Plant Control Design Handbook	ITER_D_27LH2V	7.1
[AD47]	ITER Operational States	ITER_D_54L85L	2.2
[AD48]	ITER Investment Protection Handbook	ITER_D_3VUMVW	5.0
[AD49]	Management of Local Interlock Functions	ITER_D_75ZVTY	6.0
[AD50]	Instructions for ITER System Load Specifications	ITER_D_33TTPJ	3.3
[AD51]	Instructions for Structural Analyses	ITER_D_35BVV3	4.1

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[AD52]	Instructions for Seismic Analyses	ITER_D_VT29D6	2.0
[AD53]	CAD Manual 01 - Instruction for Use and Introduction	ITER_D_AHFDDK	1.4
[AD54]	ITER Research Plan (IRP) - Level 1 - ITER Research Plan	ITER_D_24QSG6	2.0
[AD55]	MQP L3 Identification of Occupational Health & Safety Requirements related to Design	ITER_D_TME48W	2.3
[AD56]	MQP L2 Risk and Opportunity Management Procedure	ITER_D_22F4LE	6.4
[AD57]	MQP L0 ITER Policy on Safety, Security and Environment Protection Management	ITER_D_43UJN7	4.0
[AD58]	MQP L3 Contractor Safety Management Procedure	ITER_D_Q2GBJF	1.4
[AD59]	Health Protection and Safety General Coordination Plan - ITER Construction Site - Volume 0 - General Safety Rules	ITER_D_2NUEYG	6.0
[AD60]	Internal Regulations	ITER_D_27WDZW	3.1
[AD61]	Environmental requirements	ITER_D_97WRFP	2.2
[AD62]	MQP L2 ITER Site access Procedure	ITER_D_S3893D	3.3
[AD63]	Provisions for Implementation of the Generic Safety Requirements by the External Actors/Interveners	ITER_D_SBSTBM	2.3
[AD64]	MQP L3 Procedure for Occupational Health and Safety Hazard Identification and Assessment	ITER_D_AJLQRF	6.0
[AD65]	Vehicle Access and Traffic Circulation and Parking on the ITER Site	ITER_D_N3MG3V	3.2
[AD66]	MQP L2 Physical Security Protection Management Procedure	ITER_D_TZYDJH	2.2
[AD67]	ITER Site Permit to Work Procedure	ITER_D_3E8289	5.3
[AD68]	Cleanliness strategy	ITER_D_WW78E8	2.1
[AD69]	Template of Final Acceptance Certificate for PA Items	ITER_D_4QPP9E	1.1
[AD70]	Codes and Standards for ITER Mechanical Components	ITER_D_25EW4K	5.0
[AD71]	ITER Coordinate Systems	ITER_D_2A9PXZ	3.7
[AD72]	ITER Coordinate System and Coils Polarities	ITER_D_QRUDS6	1.1
[AD73]	Safe Access for Maintainability	ITER_D_RUGWUK	1.4
[AD74]	Application of the FRS Simplified Methodology to Building 13 - PBS 63.13 Assembly Building	ITER_D_RW33SG	1.1
[AD75]	MQP L2 Procedure for the CAD management plan	ITER_D_2DWU2M	2.3
[AD76]	Procedure for ITER CAD Data Exchanges	ITER_D_2NCULZ	4.2
[AD77]	Diagrams and Drawings Management System Working Instruction	ITER_D_KFMK2B	2.2
[AD78]	IS-22-41-003	ITER_D_5XL6W4	1.3
[AD79]	IS-26.CC.2A-41-001 Interface between PBS26.CC.2A and Coil Power Supply & Distribution (PBS 41)	ITER_D_DABD6D	1.7
[AD80]	IS-41PPAJ-41_IVCPowerSupplies-001	ITER_D_DY6EG9	1.1
[AD81]	IS-41-41-003 Interface Sheet between VS3 Power Supply (41.V3) and VS3 Busbars (41.V3.BB / 41.V3.BE)	ITER_D_FG5WSV	1.0

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[AD82]	IS-43-41-501 Interface between LV Class IV Power Supply of SSEN and In-vessel coil power supply	ITER_D_M2WS9P	4.0
[AD83]	IS-43-41-502 Interface between Class II-IP Power Supply of SSEN (PBS 43.BR) and In-vessel coil power supply (PBS 41.EL/V3)	ITER_D_E2ZJZF	1.0
[AD84]	IS-41-45-008 – Interface between V3PS and CODAC	ITER_D_CCSGVS	1.4
[AD85]	IS-41-46-009 – Interface Sheet (IS) between V3PS Plant Interlock System of PBS41 and PBS46	ITER_D_CD899M	1.4
[AD86]	IS-47-41-005 Interface Sheet between PBS47 (PCS) and PBS 41 (CPSS – VS3) – Architecture	ITER_D_7PE9R4	1.2
[AD87]	IS-47-41-006 Interface Sheet between PBS47 (PCS) and PBS 41 (CPSS – VS3) – Requirements	ITER_D_7PEA3L	0.0
[AD88]	IS-41-62.13-001 Interface sheet between PBS41.EL, PBS41.V3 and PBS62.13	ITER_D_ 9RCYJ5	1.8
[AD89]	AB-CMAF CMM for PBS 41 in Assembly Building 13 (SRO, DT1 and DT2)	DQ7W6W	-
[AD90]	Static and Transient Magnetic Field Maps in Tokamak Building	ITER_D_3BQBVY	3.1
[AD91]	Magnetic Field Map Database Query Tool User Manual	ITER_D_53KMVD	1.4
[AD92]	ITER Structural Design Code for Buildings (I-SDCB) - Part1: Design Criteria	ITER_D_283B24	3.4
[AD93]	ITER Structural Design Code for Buildings (I-SDCB) - Part 2: Construction	ITER_D_2E2U9X	2.0
[AD94]	Engineering Technical Documentation - PBS 62.11/14/74 - Tokamak Complex - Post-Drilled Anchors (PDA) Qualification - PDA Catalog - ENG_51_TR_110031_CW	ITER_D_8Z8HNP	2.1

4.1.2   Reference Documents (RD)

Ref.	Title	UID	Version
[RD1]	ITER Plant Breakdown Structure (PBS)	ITER_D_28WB2P	2.0
[RD2]	IDP-List for the VS3 Power Supply System CDR	ITER_D_DMLT5Y	2.0
[RD3]	PF Scenario database folder	2LVUEU	-
[RD4]	ITER Control System Glossary	ITER_D_34QECT	2.0
[RD5]	CODAC Core System Overview	ITER_D_34SDZ5	7.4
[RD6]	PLC Software Engineering Handbook	ITER_D_3QPL4H	3.1
[RD7]	HMI Style Guide and Toolkit	ITER_D_3XLESZ	4.0
[RD8]	I&C cubicle internal configuration	ITER_D_4H5DW6	4.1
[RD9]	Standard PLC Template for Interlock Applications	ITER_D_SDTX28	2.0
[RD10]	Integration Kit for PS I&C	ITER_D_C8X9AE	1.2

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[RD11]	Guidelines for the Design of the Plant Interlock System (PIS)	ITER_D_3PZ2D2	5.0
[RD12]	Guidelines for PIS configuration and integration	ITER_D_7LELG4	4.0
[RD13]	PIS Operation and Maintenance	ITER_D_7L9QXR	3.0
[RD14]	Preliminary guideline for configuration of protection and protection related systems	ITER_D_BZPJUG	1.1
[RD15]	MPP RoD - IVC (In-Vessel Coils) - Power Supplies	ITER_D_9E36DN	1.1
[RD16]	RAMI Analysis How-To Guidance	ITER_D_424JAH	1.1
[RD17]	Template for RAMI Analysis Summary Reports	ITER_D_2N3SS9	6.1
[RD18]	ITER Procedure for Performing Hazard and Operability	ITER_D_2F5L5M	2.3
[RD19]	ITER Concept of Operations	ITER_D_S7T73E	2.3
[RD20]	IO termination catalogue	ITER_D_TX7Y23	1.6
[RD21]	Conceptual I&C Diagram for VS3 Power Supply System	ITER_D_EEKZGH	2.0
[RD22]	ITER catalogue for I&C products - Cubicles	ITER_D_35LXVZ	4.2
[RD23]	ITER catalogue for I&C products - Slow controllers PLC	ITER_D_333J63	6.4
[RD24]	Catalogue for I&C products – Fast controllers	ITER_D_345X28	2.8
[RD25]	I&C cubicle internal configuration	ITER_D_4H5DW6	4.1
[RD26]	CODAC interface folder	2DF6RT	-
[RD27]	CPS SDN communication signal list	ITER_D_3LE3E2	2.4
[RD28]	Procedure for the SIL determination of the Occupational Safety I&C functions	ITER_D_MTXV7V	1.0
[RD29]	Guideline to manufacture NPE N2 or N3 cat 0 & PE cat 0	ITER_D_VHC4YM	1.3
[RD30]	Guideline for Structural Integrity Report	ITER_D_35QTKD	2.1
[RD31]	Overall occupational safety design for CPSD	ITER_D_UAMZ4U	1.1
[RD32]	HIRA of 41.IVC power supplies system	ITER_D_A6ZQSD	1.1
[RD33]	ITER_41V3BB_CBD_001: In Vessel Busbar Diagram	ITER_D_QSJJ23	5.0
[RD34]	Interface Control Document (ICD) between Coil Power Supply and Distribution (PBS 41) and In-Vessel Coils (PBS 15-IV)	ITER_D_3MSYPA	1.4
[RD35]	IS-15.IV-41-001	ITER_D_JK87TY	3.1
[RD36]	IS-41.V3-44-001 Interface sheet between VS3 Power Supply (PBS 41.V3) and Cable Tray System (PBS 44)	ITER_D_ELVTJ7	1.4
[RD37]	Deviation Request Template	ITER_D_2LRNQP	4.0
[RD38]	Template for SDR Input Data Package	ITER_D_TWW7AY	4.1
[RD39]	Site Plan - ITER Site Map	37UASM	-
[RD40]	Preliminary concept of the grounding of PBS41 ELM and VS3 components in B13 for CDR design purposes	ITER_D_92PFYU	1.2
[RD41]	Manual of CAD folder	2FQDLM	-
[RD42]	Template for ITER System Load Specifications	ITER_D_2PW74P	1.5

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[RD43]	Naming and Numbering of CPSS Components	ITER_D_DZE6SA	2.3
[RD44]	IVC impedance	ITER_D_3UZVQ5	1.5
[RD45]	Follow-up electromagnetic analysis of the ITER VS3 coil system under faulty-turns conditions	ITER_D_6VWRWS	1.1
[RD46]	VS3-PS Electrical load impedance for conceptual design	ITER_D_DMLRC5	1.3
[RD47]	Transient Operation of VS3 System Including Inductive Coupling to Passive Structure	ITER_D_VXWY3N	1.0
[RD48]	In-vessel coil currents and fusion power scenarios for the evaluation of the in-vessel coils fatigue lifetime	ITER_D_SQFNJF	1.1
[RD49]	DINA simulation of 15MA DT scenario: DINA2015-05 (Nominal-VS scenario)	ITER_D_RTXDHY	1.1
[RD50]	ITER_41V3_SLD_001	ITER_D_EEFCAW	2.1
[RD51]	Preliminary Signal Diagram of VS3 Busbar temperature sensors and flow switches	ITER_D_EEL6A2	1.5
[RD52]	Preliminary Signal List of VS3 Busbar temperature sensors and flow switches	ITER_D_EEL8RT	1.2
[RD53]	PBS41 IVC Busbars - justification for penetration integrity in case of cooling loss in busbars	ITER_D_ALNXQ2	1.1
[RD54]	26CC2A-PID-001	ITER_D_YU3V6M	32
[RD55]	Construction Design - Building 13 - Assembly Tooling Anchor Design- ENG_50_CR_130005_CW_v02.0	ITER_D_LBZRRT	1.0
[RD56]	ENG_50_DW_130002_CW - Construction Design - PBS 62.13 Laydown and Assembly Building - General Arrangement - Plan on Foundations - Sheet 1 - ENG_50_DW_130002_CW_	ITER_D_CAUSD9	6.0
[RD57]	Construction Design - PBS 62.13 Laydown and Assembly Building - General Arrangement - Tooling Anchors and Details - ENG_50_DW_130119_CW	ITER_D_LZG2TA	1.0
[RD58]	Record of decision on the Strategy for implementing and controlling disconnectors in the ELM Power Supplies system	ITER_D_AQLBG9	1.1
[RD59]	Technical Specification for Design and Manufacture of ITER IVC Busbar	ITER_D_V6EFKK	1.4
[RD60]	Amendment to the Technical Specification of IVC Busbar Contract 4300001816 to include new VS3 Extension Busbar	ITER_D_BZATA4	1.2
[RD61]	Interface Control Document (ICD) between Coil Power Supply and Distribution (PBS 41) and In-Vessel Coils (PBS 15-IV)	ITER_D_3MSYPA	1.4
[RD62]	Interface Control Document (ICD) between Plant Installation Tooling (PBS-22) and Coil Supply & Distribution (PBS-41)	ITER_D_33ACF8	1.1
[RD63]	Interface Control Document (ICD) between Component Cooling Water System (PBS-26CC) and Coil Power Supply & Distribution System (PBS-41)	ITER_D_2FPYX7	2.3

[RD64]	Interface Control Document between PPEN (PBS41.PP) and AC/DC Converters (PBS41.xx)	ITER_D_2KSK3W	4.0
[RD65]	ICD-41-43 Interface Control Document for Steady State Electrical Network (PBS 43) and Coil Power Supply and PPEN (PBS 41)	ITER_D_35BQZA	1.4
[RD66]	Interface Control Document between Coil Power Supply and Distribution (PBS 41) and Cable Tray Systems (PBS 44)	ITER_D_CGQ4PD	2.0
[RD67]	ICD-41-45 Interface Control Document for Coil Power Supply & Distribution (PBS 41) and CODAC (PBS 45)	ITER_D_2NKSW9	3.0
[RD68]	ICD-41-46 Interface Control Document for Coil PS & Distribution (PBS 41) and Central Interlock System (PBS 46)	ITER_D_2M58GX	4.0
[RD69]	ICD-41-47 Interface Control Document for for Plasma Control System (PBS 47) and Coil Power Supplies & Distribution (PBS 41)	ITER_D_ 33KFL9	4.1
[RD70]	Interface Control Document (ICD) between Coil Power Supply and Distribution (PBS41) and Assembly Building (PBS62.13)	ITER_D_9MPWW6	2.6

4.2 Applicable Codes and Standards

It is the responsibility of the DA to procure the relevant Codes and Standards applicable to the scope of this Technical Specification. The latest applicable versions of Codes and Standards shall be referenced.

Ref.	Code	Title
[CS1]	IEC 60076	Power transformers
[CS2]	IEC 60146	Semiconductor converters
[CS3]	IEC 60747	Semiconductor devices
[CS4]	IEC 61071	Capacitors for power electronics
[CS5]	IEC 60071	Insulation coordination
[CS6]	IEC 60664	Insulation coordination for equipment within low-voltage supply systems
[CS7]	IEC 62477-1	Safety requirements for power electronic converter systems and equipment - Part 1: General
[CS8]	IEC 61508	Functional safety of electrical/electronic/programmable electronic safety-related systems
[CS9]	IEC 61511	Functional safety - Safety instrumented systems for the process industry sector

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[CS10]	IEC 61000-3-6	Electromagnetic compatibility (EMC) - Part 3-6: Limits - Assessment of emission limits for the connection of distorting installations to MV, HV and EHV power systems
[CS11]	IEC 61000-4-4	Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test
[CS12]	IEC 61000-4-5	Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test
[CS13]	IEC 61000-6-2	Electromagnetic compatibility (EMC) - Part 6-2: Generic standards - Immunity standard for industrial environments
[CS14]	IEC 61000-6-4	Electromagnetic compatibility (EMC) - Part 6-4: Generic standards - Emission standard for industrial environments
[CS15]	IEC 61204-3	Low-voltage switch mode power supplies - Part 3: Electromagnetic compatibility (EMC)
[CS16]	IEC 60947	Low-voltage switchgear and controlgear
[CS17]	IEC 62271	High-voltage switchgear and controlgear
[CS18]	IEC 60502	Power cables with extruded insulation and their accessories for rated voltages from 1 kV (Um = 1,2 kV) up to 30 kV (Um = 36 kV)
[CS19]	IEC 60529	Degrees of Protection Provided by Enclosures (IP Code)
[CS20]	IEC 60068	Environmental testing
[CS21]	IEC 60034	Rotating electrical machines
[CS22]	IEC 61800-5-1	Adjustable speed electrical power drive systems - Part 5-1: Safety requirements
[CS23]	IEC 61936-1	Power installations exceeding 1 kV AC and 1,5 kV DC - Part 1: AC
[CS24]	NF C 13-200	High voltage electrical installations
[CS25]	NF C 15-100	Low-voltage electrical installations
[CS26]	NF C 18-510	Operations on electrical network and installations and in an electrical environment
[CS27]	2006/42/EC	Machinery Directive
[CS28]	2011/65/EU	Directive of the European Parliament and of the Council on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) in the European Regulation
[CS29]	2014/30/EU	Directive of the European Parliament and of the Council of 26 February 2014 on the harmonisation of the laws of the Member States relating to electromagnetic compatibility
[CS30]	2014/35/EU	Low Voltage Directive
[CS31]	2014/68/EU	Pressure Equipment Directive (available: ITER_D_RZ6PAK)
[CS32]	517/2014	Regulation (EU) of the European Parliament and of the Council on fluorinated greenhouse gases
[CS33]	EN 1990	Eurocode 0: Basis of structural design

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[CS34]	EN 1991	Eurocode 1: Actions on structures
[CS35]	EN 1993	Eurocode 3: Design of steel structures
[CS36]	EN 1998	Eurocode 8: Design of structures for earthquake resistance
[CS37]	ASTM D5144	Standard Guide for Use of Protective Coating Standards in Nuclear Power Plants
[CS38]	ANSI/AISC 360	Specification for Structural Steel Buildings
[CS39]	EN 1090	Execution of steel structures and aluminium structures
[CS40]	EN ISO 12944	Corrosion Protection of Steel by Protective Paint
[CS41]	EN ISO 1461	Hot dip galvanized coatings on fabricated iron and steel articles. Specifications and test methods
[CS42]	EN ISO 8501	Preparation of steel substrates before application of paints and related products – Visual assessment of surface cleanliness

5 Scope of Supply, Classifications and Design Basis

This section defines the scope of supply and describes the responsibilities for each physical connection point on the boundary of supply and installation. The system and component classifications are provided, as well as the design basis conditions and events.

5.1 Scope of Supply

The scope of supply shall comprise the execution of the turnkey project for the VS3 Power Supply System. This includes, without limitation, the engineering design, manufacturing, factory and site testing, delivery, installation, system integration, and commissioning of all related components and subsystems.

The system development lifecycle shall be performed in compliance with all applicable IO procedures, not limited to those listed in section 13. The resulting documentation shall be considered as integral part of the scope of supply.

The VS3 Power Supply System delivered under this procurement shall comply fully with all performance requirements and technical specifications set forth in this Technical Specification.

Table 5-1 lists the main systems, structures and components in the scope of supply. Not listed are all auxiliary equipment and components needed to obtain a fully operational system as per the requirements of this document.

Table 5-1: scope of supply – main systems, structures and components

Qty	Component	Main characteristics
2	Power Converter, comprising:	1.2 kV, 80kA pk
	- Step-down transformer	22 kV primary
	- Active Front-End Rectifier	1.2 kVdc, 1.75 MW
	- Energy Storage Capacitor Bank	1.2 kV, ≥12 MJ
	- DC Link Fast Discharge Unit	1.2 kV, ≥12 MJ
	- Inverter	1.2 kV, 80 kApk
	- Disconnector, bypass and earthing switches	
	- Earthing resistors and monitoring	
	- Local I&C	
2	Crowbar assemblies	1.2 kV, 120kA pk
1	Dummy Load	2.4 kV, 80kA pk
1	Plant I&C system	
1	Main Steel Structure	Up to 35 x 19 x 11 m envelop

The scope of supply explicitly includes all associated design and manufacturing documents and all source code of I&C software.

5.2 Physical Connection Points on Boundaries of Supply and Installation

This section describes the physical connection points and associated responsibilities at the interface between IO supplied equipment and DA supplied equipment. The mechanical- or structural-related interface points, as defined in section 10 on e.g. anchoring and fixation, are not addressed in this section.

Pertaining to the responsibilities at physical connection points, the following principle applies:

1. Where the connection points are located on/at components or systems of IO, the DA is responsible for the connection of their SSC's.
2. Where the connection points are located on/at components or systems supplied by DA, IO is responsible for the connection of their SSC's.

The physical connection points currently foreseen are listed in Table 5-2. For any physical connection points, the above general principle applies unless otherwise agreed between the parties.

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Table 5-2: Physical connection points and responsibilities on boundaries of supply and installation

		Responsibilities		
PBS	Interface type	Supply	Connection	Connection Point Description
26	Cooling Water System *Counter flanges of cooling water pipes*	IO	DA	The PBS 26 counter flanges are the interface points to which DA shall weld their cooling pipes. IO provides the counter flanges.
41.V3.BE	VS3 Extension Busbars *Busbar terminals and flanges*	IO	DA	The busbar terminals are the interface points to which DA shall connect their conductors connecting to the power supply output. The DA shall supply and install the enclosures covering the connections, which shall be adapted to the flanges of 41.V3.BE.
41.V3.BE 41.V3.BB	VS3 Extension Busbars *I&C Interface*	DA	IO	The wire terminals in the I&C cubicle supplied by DA are the interface point to which IO shall connect the sensor cables originating from B11-L4.
41.EL.MV	Feeder cells of ELM-PS MV Substation *Power and I&C interface*	IO	DA	The downstream terminals inside the feeder cells and the downstream relay, protection and monitoring terminals are the interface points to which DA shall connect their AC feeder and I&C cables, respectively. The DA is also responsible for the routing and installation of the cables in coordination with PBS 44.
43	LV Distribution Board / Cubicles *Power Interface*	DA	IO	The upstream terminals of the incoming line circuit breakers / disconnectors are the interface points to which IO shall connect their LV supply cables. IO is equally responsible for the upstream cable trays/conduits where required.
44	Cable Tray System			Refer to section 9.9
45, 46	I&C Cubicles and Network Switches *Interface with Central I&C System*	DA	IO	The network switches inside the I&C cubicles supplied by DA are the interface points to which IO shall connect their central I&C network and signal cables. Sufficient space shall be reserved within the cubicle to allow IO to install any required fibre-optic cassettes.
62.13	Water Drainage System *Physical Interface*	IO	DA	The drainage channel in the B13 slab is the physical interface point to which DA shall connect their piping for the discharge of water, if any.

5.3   System and Components Classification

This section defines the classification of the components, in accordance with [AD4].

5.3.1   Quality Classification

The quality classification is as follows:
- VS3-PS System (excl. Crowbar): QC-3
- VS3-PS Crowbar System: QC-2

All components that contribute to interlock functions requiring a 3IL-3 integrity level are classified as QC-2, refer to section 6.4.

Individual parts used to fabricate the VS3 Power Supply are classified as QC-4.

For QC-2 subsystems and components, the DA shall use the Manufacturing Database (MDB) provided by IO to monitor inspection plans.

5.3.2   Safety Classification

The VS3 Power Supply System is classified as NSR (Non-SIC).

Nuclear Safety requirements are included in section 12.

5.3.3   Seismic Classification

The seismic classification of the VS3 Power Supply System is defined as: SC-2.

5.3.4   Pressure Equipment Classification

The piping and cooling water networks are subject to the 2014/68/EU Pressure Equipment Directive [CS31].

The cooling water networks of VS3-PS are classified as PE category 0.

The associated design guidelines, including usable codes for the design and manufacture of PE cat. 0, are given in [RD29].

5.4   Design Basis Conditions and Events

The VS3-PS components shall be designed, constructed and qualified through a qualification program that shall demonstrate that each component is able to perform its functions or remain stable in all normal and accidental conditions and events foreseen for its functioning as described in the load specification [AD38].

The demonstration can be done through analysis, tests, relevant operational experience or a combination of those. In particular, the VS3-PS system function and performance shall be tested in accordance with the test requirements set out in section 15.

TECHNICAL REQUIREMENTS

6 Operational Requirements

The global operational requirements for the VS3 Power Supply are listed in this section. Specific technical requirements for the various subsystems are listed separately in chapter 7.

6.1 Performance requirements

The VS3 Power Supply shall support three distinct operating regimes, between which it shall be able to transition seamlessly and uninterruptedly:

1. Continuous operation – vertical stabilization "noise"
2. Pulsed operation – any pulse of 1 to 90 sec, e.g. during plasma ramp-up and ramp-down
3. VDE Pulse operation – any pulse up to 1 sec and up to peak current, for VDE mitigation

The VS3 Power Supply shall support three electrical load configurations:

1. Operation on VS coils in 8-turn configuration
2. Operation on VS coil in 6-turn configuration
3. Operation on VS3-PS dummy load

6.1.1 Power Supply Output requirements

This section covers the requirements related to the output of the power supply. Here, the power supply output is defined as the point where the power supply is connected to the VS3 Extension Busbar.

The performance requirements of the power supply are listed in Table 6-1, which summarises the requirements set out in the forthcoming subsections.

Table 6-1: VS3-PS output performance requirements

	6-turn	8-turn	Unit	Conditions
Output voltage				
Range [1]	-2400 … 2400		V	Under no-load conditions
Transient response time	≤ 1		ms	From the receipt of a 100% step change to the output voltage reaching 90%, under no-load conditions
Discharge time	< 60		s	Without load
Output current				
Continuous operation	4.0	3.0	kA rms	Indefinitely, including instantly after pulse
Pulsed operation	$1.3 \cdot 10^9$	$0.8 \cdot 10^9$	A^2s	Any pulsed operation for 1...90 seconds
VDE pulse operation	80	60	kA pk	
Current ripple (pk-to-pk)	≤ 10		A	At nominal load [2]
VDE Pulse operation				
Pulse duration	≤ 1		s	

Repetition rate	10	s
Events per Tokamak pulse	≤ 3	pulses
Pulsed operation		
Pulse duration	≤ 90	s
Time between pulses	≥ 10	s
Events per Tokamak pulse	≤ 2	pulses

Note 1: the voltage range under nominal load conditions is implicitly defined by the required output current waveforms
Note 2: nominal load refers to the load impedance of the respective VS coil turn configuration

6.1.1.1 Output voltage

The VS3 Power Supply shall be capable of providing bipolar output voltage, with seamless polarity reversal, up to ±2.4 kV under no-load conditions.

The output voltage range, under nominal load conditions, shall be sufficient for realizing the required output current waveforms.

The transient response time of the output voltage for a 0-100% voltage step change shall be 1 millisecond or less, from receiving the corresponding control command by the VS3-PS Plant Controller to voltage reaching 90% at the power supply output, under no-load conditions.

The output voltage regulation bandwidth (-3dB) shall be at least 250 Hz for large-scale variations (0-100%), and at least 500 Hz for small-scale variations (10% variation of rated voltage).

The output stage shall be discharged and de-energized in 60 seconds or less, independent of load conditions and including no-load condition.

6.1.1.2 Output current

The VS3 Power Supply shall be capable of supplying bidirectional current, with the continuous and pulsed current rms values and durations shown in Figure 6-1.

The output current regulation bandwidth (-3dB) for large-scale variations (0-100%) shall be at least 5 Hz under nominal load conditions.

The requirements for the three operating regimes are detailed in the forthcoming subsections.
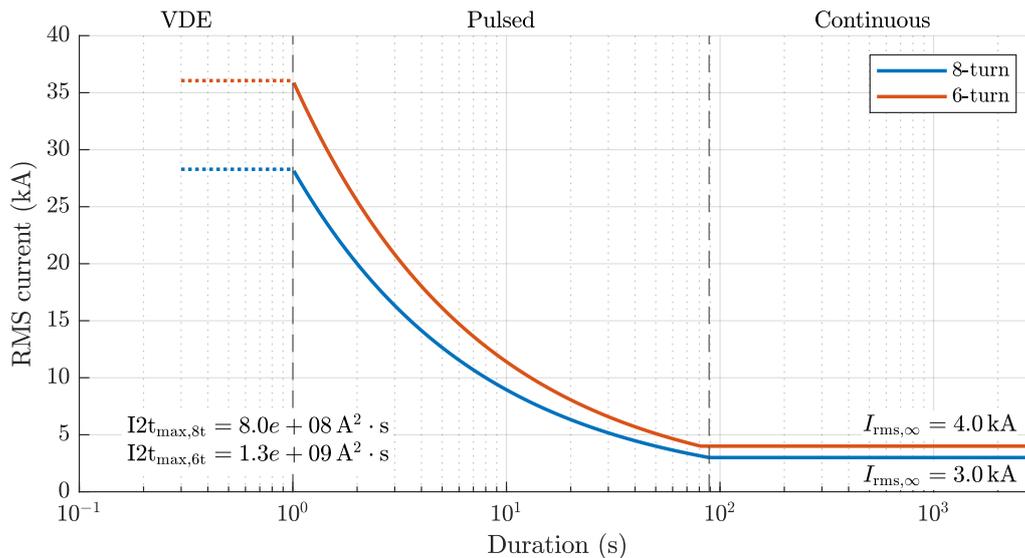
Figure 6-1: required operating root mean square current levels as a function of the pulse duration. The VDE pulse regime (dashed lines) is covered by separate requirements.

It is the responsibility of the VS3-PS to limit the externally provided setpoints and/or the power supply output to ensure operation within the design limits; the IO's interfacing system(s) have no responsibilities in regard to ensuring the power supply is not operated outside of its design space.

6.1.1.2.1 Continuous operation – "noise"

The VS3-PS shall be capable of supplying the regular vertical stabilization current ("noise") for an indefinite period of time, irrespective of any earlier or directly preceding pulses.

The dynamics of this operating regime are characterised by the growth rate of the plasma's vertical instability and the noise in the vertical velocity measurement from diagnostics, which has an estimated rms value of 0.6 m/s with uniform power spectrum (white noise) in the frequency band [0, 1 kHz]. A representative operating waveform is provided in Nominal-VS scenario "15MA DT-DINA2015-05" [RD49], which is listed in [RD48].

The dynamics required for VS noise operation are covered by the requirements on voltage regulation bandwidth, which in combination with the circuit impedance defines the achievable current levels.

6.1.1.2.2 Pulsed operation

Pulsed operation is defined as supplying any pulse with a duration between 1 and 90 seconds and an RMS value exceeding the continuous output current rating. Such pulses may occur for instance during plasma ramp-up and ramp-down phases. Any pulse with duration less than 1 second is considered a VDE pulse with the associated requirements.

The VS3 Power Supply shall be capable of supplying current pulses into the load with a duration ranging from 1 to 90 seconds and with an I^2t value of $8 \cdot 10^8$ A^2·s or $13 \cdot 10^8$ A^2·s for respectively 8-turn and 6-turn operation, refer to Figure 6-1. The performance requirements for the pulsed operation mode are to be considered fully enveloped by the performance capabilities specified for noise and VDE pulse operation.

The required duty is up to two pulses per Tokamak pulse, with a minimum of 10 seconds between subsequent (VDE or Pulsed) current pulses for recharging the DC link and thermal relaxation.

6.1.1.2.3 VDE pulse operation

The VS3 Power Supply shall be capable of supplying VDE current pulses into the load circuit comprising the 6-turn or 8-turn VS coil configuration with current amplitudes up to 80 kA and 60 kA, respectively.

The possible VDE pulse current waveforms are enveloped by the following expression, which comprises two superimposed exponentials with distinct time-constants for the rise and fall intervals:

$$i_{VDE}(t) = A \cdot \left(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}} \right)$$

The above expression shall be considered in conjunction with the following parameters:
- Amplitude
  - $A = 74.4$ kA for 8-turn operation
  - $A = 99.2$ kA for 6-turn operation
- Time-constant $\tau_1 = 16$ ms
- Time-constant $\tau_2 = 304$ ms

The corresponding waveforms are shown in Figure 6-2.
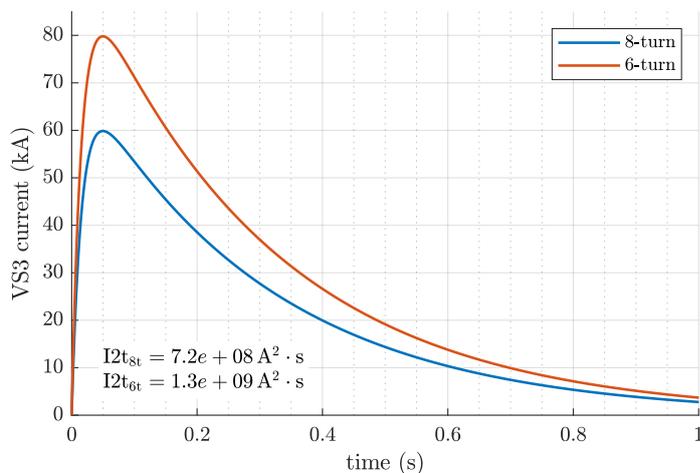
Figure 6-2: definition of enveloping current waveform for VDE pulse operation

The required duty is up to three pulses per Tokamak pulse, with a minimum repetition time of 10 seconds, allowing for recharging the DC Link and thermal relaxation. It is expressly pointed out that the VDE pulse duty is additional to the generic Pulsed operation. Nevertheless, a minimum of 10 seconds is permitted between pulses of different type (i.e. the power supply is only required to deliver a full-performance VDE current pulse 10 seconds after completion of the generic pulsed current).

The feasibility of the rise time implied in Figure 6-2 in regard to the defined output voltage and the impedance/time-constant of the VS3 coil circuit will be addressed at later stage.

6.1.1.3 Operating area

The VS3 Power Supply shall be capable of 4-quadrant operation, allowing to sink/source energy from/to the connected load in both current directions.

6.1.1.3.1 Operating profile

An example operating profile under the foregoing requirements is provided in Figure 6-3. This waveform is referred to as 3VDE waveform and represents a possible worst design case under the foregoing performance requirements.
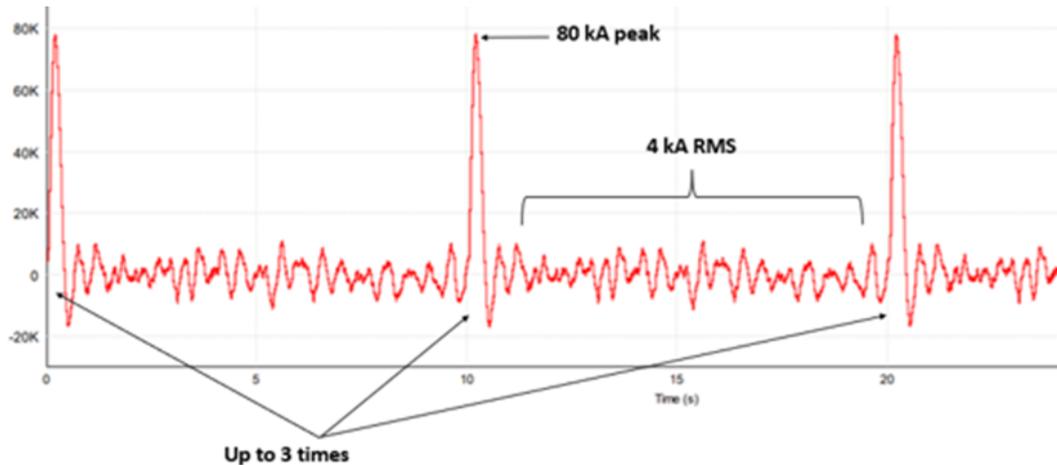
Figure 6-3: example waveform of VDE pulses amidst continuous noise operation

6.1.1.4 Output regulation

The output regulation performance (accuracy, precision, bandwidth, etc.) of the VS3 Power Supply shall be in accordance with the values listed in Table 6-2.

Table 6-2: VS3-PS output regulation requirements

	6-turn	8-turn	Unit	Conditions
Current regulation				
Resolution	≥ 16		bits	Over full range from -Inom to +Inom
Accuracy	$\leq 1\%$		A	Over range from 2% to 95% of Inom
Line regulation	$\leq 0.5\%$ of Inom		A	For ±10% AC input voltage variation
Bandwidth (-3dB)	≥ 5		Hz	Large-scale bandwidth (0-100% of Inom), on nominal load
Voltage regulation				
Resolution	≥ 16		bits	Over full range from -Vnom to +Vnom
Accuracy	$\leq 1\%$		V	Over range from 10% to 95% of Vnom
Line regulation	$\leq 0.5\%$ of Vnom		V	For ±10% AC input voltage variation
Bandwidth (-3dB)	≥ 250		Hz	Large-scale bandwidth (0-100% of Vnom), on nominal load
Bandwidth (-3dB)	≥ 500		Hz	Small-scale bandwidth (10% variation of Vnom), on nominal load

Note 1: Inom refers to the maximum nominal output current (80 kA)

Note 2: Vnom refers to the nominal output voltage (2.4 kV)

6.1.2   Power Supply Input requirements

The VS3 Power Supply input stage shall be designed, controlled and operated to allow the output side to operate with the performance requirements as per section 6.1.1.

The performance requirements related to the input side of the power supply are listed in Table 6-3, which summarises the requirements set out in the forthcoming subsections.

Table 6-3: VS3-PS input performance requirements and compatibility

	min.	typ.	max.	Unit	Conditions
AC input					
Voltage	19.8	22	24.2	kVAC	Line voltage (phase-to-phase)
Frequency	49.5	50	50.5	Hz	Minimum operating range; larger variations are possible
THDv [1]			8%	-	Voltage Total Harmonic Distortion
AC load					
Power			3.5	MVA	
Power factor	0.95			-	Any load >10% of nom. charging power
THDi [1]			6%	-	Current THD generated by VS3-PS
Inrush current [2]			10·Inom	A	
DC Link					
Voltage		1200	1250	VDC	
Charging time (initial)			120	s	From 0V to Vdc(nom), i.e. including pre-charge
Charging time			8	s	From Vdc(min) to Vdc(nom) while providing noise current
Discharge time (bleeder)	600		2250	s	From Vdc(max) to <50V
Discharge time (fast)	5		20	s	From Vdc(max) to <50V

Note 1: refer to section 9.7.4

Note 2: refer to section 9.7.3

Note 3: Vdc(min) refers to the lowest operable DC Link voltage (no uncontrollable diode conduction)

Note 4: Vdc(nom) refers to the nominal operating voltage of the DC Link (typical value in table)

Note 5: Vdc(max) refers to the maximum DC Link Voltage that may occur at any time during operation

6.1.2.1   AC input

The VS3-PS shall be capable of operating at full performance with an AC input voltage of 22 kV ± 10%, and a frequency of 50 Hz ± 1%. Larger voltage and frequency variations are exceptionally possible, nevertheless VS3-PS is not required to operate outside the stated ranges.

The VS3-PS shall be capable of operating with the specified output performance for a Total Harmonic Distortion on the AC input voltage of up to 8%.

6.1.2.2   AC load

The instantaneous AC input power required by VS3-PS shall not exceed 3.5 MVA.

The power factor of VS3-PS shall be equal to or better than 0.95 for any loading condition above 10% of the nominal charging power.

The Total Harmonic Distortion of the AC-side current generated by VS3-PS shall not exceed 6%.

The inrush current, including transformer magnetisation currents and (pre)charging of the DC Link, shall not exceed 10 times the nominal AC-side current.

6.1.2.3   DC Link

The VS3-PS shall be designed, controlled and operated for a nominal DC Link voltage of 1200 V for each power converter. The DC Link voltage shall not exceed 1250 V at any time during operation.

The VS3-PS shall be capable of charging the DC Link from a de-energized state, hereinafter referred to as initial charging, to the nominal DC Link voltage in 120 seconds or less. This duration includes the pre-charging operation.

The VS3-PS shall be capable of (re)charging the DC Link from Vdc(min), the minimum operable DC Link voltage at which the input stage meets all input requirements, to the nominal voltage in no more than 8 seconds.

The VS3-PS shall be equipped with a fast discharge mechanism that is capable of discharging the DC Link including Energy Storage Capacitor Bank from the maximum voltage to a voltage of 50V or below in less than 20 seconds, nevertheless with a minimum duration of 5 seconds.

6.2   Operating requirements

6.2.1   Output control modes

The VS3 Power Supply shall be capable of providing the following output control modes, which are further detailed in the below subsections:
- Closed-loop current control
- Closed-loop voltage control

For this purpose, the VS3 Power Supply controller shall accept the following input signals:
1. Output control mode
2. Output voltage/current setpoint

The setting of the output control mode shall be allowed remotely via the interface with ITER's Central I&C system.

6.2.1.1 Closed-Loop Current Control

The VS3 Power Supply shall be capable of closed-loop current control to follow a current command, resulting in the output current regulation performance listed in Table 6-2.

6.2.1.2 Closed-Loop Voltage Control

The VS3 Power Supply shall be capable of closed-loop voltage control to follow a voltage command, resulting in the output voltage regulation performance listed in Table 6-2.

This voltage control mode is foreseen for most operation under the control of PCS, in which case PCS provides voltage setpoints to VS3-PS and performs its own closed-loop current control.

6.2.2 Operating and Service Life Requirements

The VS3 Power Supply shall be designed for the operating and service life requirements summarized in Table 6-4 and further detailed in the forthcoming subsections.

Table 6-4: operating and service life requirements

Parameter	Value			Remarks
Design life	$\geq$ 20 years			
Number of Tokamak pulses	$\geq$ 30,000			
Tokamak pulse repetition time [Note 1]	$\leq$ 1800 s for $t_{burn} \leq$ 450s			PR907-R [AD3]
	$\leq 4*t_{burn-1}$ for $t_{burn} >$ 450s (i.e. duty cycle $\geq$ 25%)			
Tokamak <u>burn</u> time t_{burn} (typ.) [Note 2,3]	Inductive operation	450 s	(TBD) %	PR515-R [AD3]
	Hybrid operation	1000 s	(TBD) %	
	Non-inductive operation	3000 s	(TBD) %	
Tokamak burn time (max.)	3600 s			PR5352-R

Note 1: t_{burn-1} denotes the burn time of the previous pulse
 	
Note 2: VS3-PS needs to be operating not just during the flat-top, but for the entire Tokamak pulse duration, which comprises the following intervals:
    - Ramp-up: increase of plasma current (typically 10-100s)
    - Flat-top: static plasma current (comprising entry, burn, exit)
    - Ramp-down: decrease of plasma current to zero (typically 3 times ramp-up time)
Note 3: Distribution of operating scenarios as per TBD				

6.2.2.1 Design Life

The VS3 Power Supply shall be designed for an operating lifetime no less than 20 years.

6.2.2.2 Number of pulses

The VS3 Power Supply shall be capable of operating for at least 30,000 Tokamak pulses, accumulated over which the VS3-PS shall be capable of providing a minimum of 30,000 VDE pulses at full current level under the specifications in section 6.1.1.2.3, and, in addition, a minimum of 60,000 current pulses at full I^2t level under the definition of Pulsed operation and the associated specifications in section 6.1.1.2.2.

6.2.2.3 Pulse Duration and Repetition Rate

The VS3 Power Supply shall be capable of operating at full performance levels for the plasma pulse durations in Table 6-4 and the repetition rates described in PR907-R of [AD3], which states:

During any plasma operation phase, ITER shall perform a minimum of 2 Tokamak pulses per hour (i.e. the Tokamak pulse repetition time* shall be 1800 s or less), with the following exceptions:

- *For burns longer than 450 s, the Tokamak pulse repetition time* shall be a maximum period of 4 times the duration of the previous pulse, i.e. the Tokamak pulse duty cycle shall be 25% or more.*
- *For DT-1:*
  - *For Q = 10 / 300 s burns, ITER shall be able to perform a minimum of 1 Tokamak pulse per hour.*
  - *For lower Q values (for any burn duration), several pulses per hour may be possible, in line with the fuel recycling capacity as specified in Section 4.1.7.7.*
- *For any plasma scenario during DT-2, the Tokamak pulse duty cycle ≥ 25% for burns > 450 s will be achieved by operating with the fuel recycling capacity specified in Section 4.1.7.7.*
- *Note that:*
  - ** The repetition time between Tokamak pulses is defined as the time between the start of a Tokamak pulse and the start of the next Tokamak pulse.*
  - *For non-DT plasmas (i.e. no burns), the "burn durations" quoted in this requirement must be considered as "pulse flat-top durations" (see Table 4.1).*

6.2.2.4 Design Operating Schedule

The VS3 Power Supply shall be designed to be capable of operating for periods of 11 consecutive days while accommodating three-shift daily plasma operation, followed by 3 days of routine maintenance.

The VS3 Power Supply shall be designed so that plasma operation can be conducted for periods of up to 16-months continuously in three 8-hours work-shift daily operating mode to perform the following actions: plasma operations, test, conditioning, routine maintenance.

The design of the VS3 Power Supply shall not preclude the possibility of remaining de-energized for prolonged periods of time (e.g. up to 5 years), after which it shall not require significant restart, regeneration or recommissioning procedures.

6.2.3   Termination of operation

At any time, VS3-PS shall be able to terminate the ongoing operation, thus aborting the semiconductor switching and the supply of current/voltage to the load, within 5 ms after receipt of the corresponding signal.

The magnetic energy stored in the VS3 coil circuit shall be appropriately discharged.

The DA shall propose the strategy with respect to the discharge of the excess magnetic energy in the VS3 coil circuit following an expected or unexpected shutdown, taking into consideration all operational and other relevant requirements in this technical specification, subject to acceptance of IO.

For illustrative purposes, such strategy may, among others, be based on:
- Shunting the VS3 coil circuit for resistive self-discharge, using e.g. the crowbar system
- Discharging the VS3 coil circuit into DC Link e.g. through integrated diodes in inverter legs, supplemented by:
    o Regeneratively injecting the DC Link's excess energy into the AC grid
    o Dissipating the DC Link's excess energy in a resistive element

The need for discharge of the DC Link shall be assessed for all relevant termination scenarios, including faults, and shall be addressed in the framework of the FMECA (refer to section 6.5).

For all unexpected shutdown events, e.g. due to faults or loss of services, the recovery time after a termination event shall not exceed 30 minutes. For expected events, such as controlled terminations, the recovery time after such event shall not exceed 2 minutes.

6.2.4   Pulse capability and status reporting

6.2.4.1   Pulse capability
The VS3 Power Supply shall continuously determine its ability to provide a full-performance VDE pulse as per the requirements of Table 6-1.

As a minimum, this assessment shall take into account the following aspects:
- the momentary operating state
- the momentary energy stored in the ESCB, comprising:
    o the momentary ESCB State-of-Charge (SoC)
    o the momentary ESCB State-of-Health (SoH)
- the momentary thermal margins of critical components

The inability to provide a full-performance VDE pulse shall not prevent another (degraded) VDE pulse from being generated and delivered to the coil circuit, up to the point where conventional and investment protections ultimately limit and respectively terminate the operation.

6.2.4.2   Status reporting
The pulse capability shall be communicated to PCS as per section 9.10.3.

6.2.5 *Plasma Control Requirements*

All specific requirements related to plasma control are included in section 9.10.3.

6.3 **Operating modes and states**

The VS3-PS I&C system operation shall be compatible and coordinated with the operation of the ITER machine and other systems according to Chapter 10 - Common Operation States of [AD47]

6.3.1 *Common Operational States (COS)*

"At all times each plant control system reports to CODAC-SUP a translation of its internal states into one COS" [AD47]. Ergo, from the central control system and the operation of ITER, only the Common Operation States of the respective plant system, i.e. VS3-PS, is displayed. This ensures a uniform view on the states of each plant system.

The COS states are:

- Shutdown
  - COS-01 Off
  - COS-13 Safe
  - COS-10 Absent
- Not Ready
  - COS-02 Not Ready
  - COS 11 Local
  - COS-12 Fault
- Ready
  - COS-03 Ready
- Starting
  - COS-04 Initializing
  - COS-05 Initialized
  - COS-09 Aborting
- Running
  - COS-06 Executing
- Post Checks
  - COS-07 Post-checks

A mapping of the plant system states to COS has to be possible at any time.
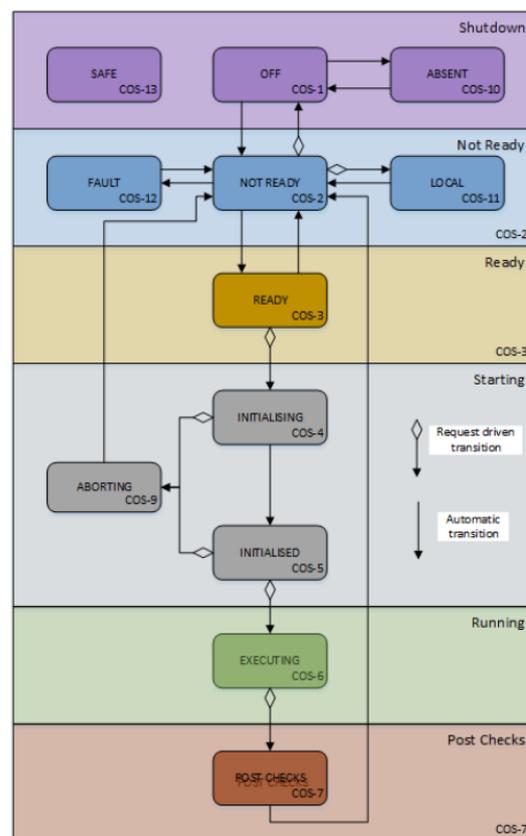
Figure 6-4: Common Operational States (COS), adopted from [AD47] − Figure 12

6.3.2   *Principal operating states*

For the plant system VS3-PS, at least four operating states shall be implemented as shown in Figure 6-5 and further detailed in Table 6-5. In each Plant Operating State (POS), specific substates can be implemented by the DA as long as a mapping to COS is possible.
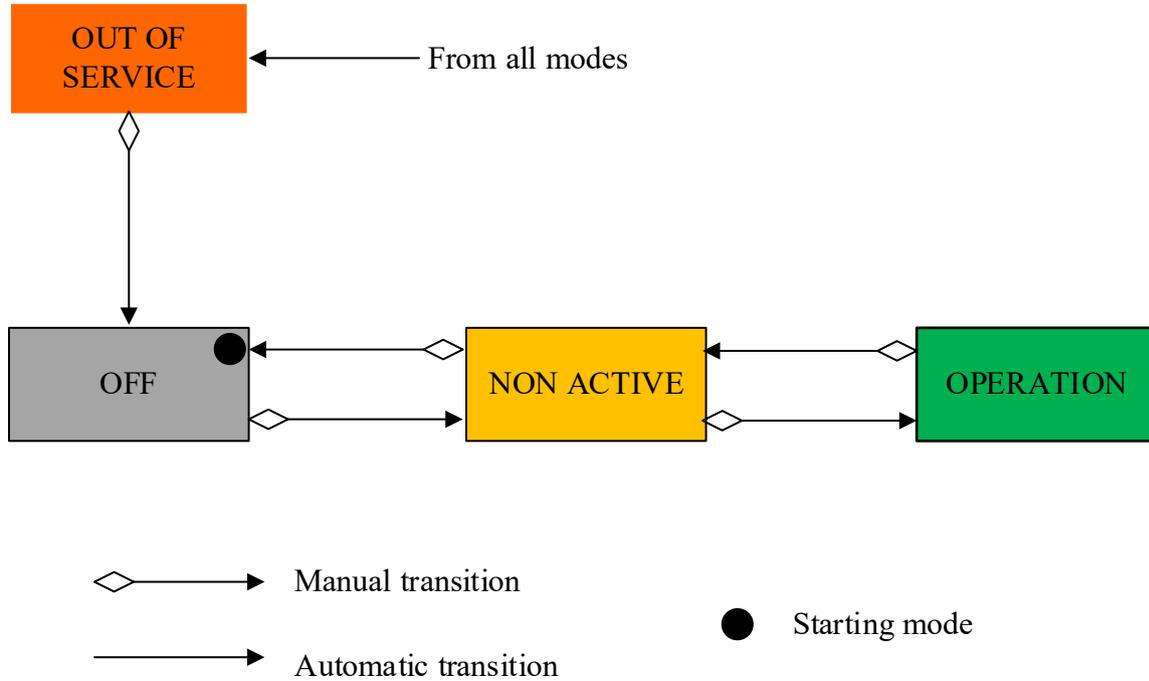
Figure 6-5: Principal plant operating states of VS3 Power Supply

Table 6-5: Description of principal plant operating states of VS3 Power Supply

Plant Operating State	Substates	Description
OUT OF SERVICE		VS3-PS is out-of-service when a compulsory shutdown is required, or when an unrecoverable internal fault has occurred that requires the permanent shutdown until the necessary maintenance or repairs have been performed.
OFF	To be defined by DA	VS3-PS is disconnected from MV grid. Most LV equipment is powered off, although I&C systems may remain powered-on depending on the level of shutdown required. This mode is typically used during maintenance or commissioning phases. The configuration of the VS3-PS is controlled locally and depends on the activities that are to be performed (tests, maintenance, repair, etc.).

NON-ACTIVE		VS3-PS is not active; all I&C and auxiliary systems are initialized and/or operational; the DC Link is de-energized.
		This mode is typically used in between plasma operations with a long period of inactivity, or when the VS3-PS is not required during physics experiments.
		Access to the VS3-PS area is not permitted and parts of the system could remain energized.
		VS3-PS I&C systems operate normally to provide measurements to and to ensure interlock functions.
OPERATION		VS3-PS is ready for operation or operational. The DC Link may be energized, and the output of the power supply may be progressively established through the substates
		In this mode, the VS3-PS system is energized and ready to deliver power to the loads, as requested by the PCS.
		VS3-PS I&C systems operate normally.
		This mode shall also consider a degraded operation in which one of the VS3-PS inverters has failed and is bypassed.

As a minimum, the following substates shall be foreseen:

Table 6-6: plant operation substates to be foreseen

Substate	Description
Tripped	VS3-PS DC Link remains energized, yet the output stage is disabled following the detection an operating condition outside of the programmed or design limits. A manual control action is required to return to the fully operational state. Typical conditions triggering the tripped state: - Overcurrent protection - Overvoltage protection When tripped, the inverter output is disabled, the inverter semiconductor switches no longer receive switching signals. The disabled inverter acts like an open circuit, as long as the coil circuit voltage remains below the DC Link voltage.
UpcomingShutdown	Specific non-critical operational or thermal conditions require the VS3-PS to shutdown within a predefined amount of time. Such conditions may include a detected absence of cooling water flow in the busbars, whereas the busbars may continue operating for a limited amount of time before overtemperature conditions arise. This substate allows any ongoing plasma operation to terminate in a controlled way.
DummyLoadOps	VS3-PS is operating on dummy load; any energization of or connection with the actual coil circuit is excluded. This substate shall be reported as COS:NotReady.

6.3.3 Human Machine Interface

The manual transitions between the operating modes and states shall be performed remotely through CODAC networks and the ITER Human Machine Interface (HMI), during test, commissioning and maintenance activities.

The plant operating states and substates of VS3-PS shall be reported to the ITER HMI using central networks.

The states and the corresponding configurations of the VS3-PS system will be defined during the execution of the task agreement.

The ITER Human Machine Interface of the COS state machine design and implementation is not in the scope of the DA. The DA is just responsible of sending, receiving and processing commands generated by the ITER HMI.

6.3.4 Reconfiguration

The VS3-PS I&C systems as well as certain actuators shall allow reconfiguring the VS3-PS systems configuration from the ITER central control room via SUP. This includes configuration changes from CIS or CODAC.

The local, manual setting of configuration parameters shall be prohibited. The configuration of interlock-related parameters shall be performed exclusively through, CIS as specified in section 6.4.2.4.

6.4 Investment Protection Functions (Interlock Functions)

This section defines the operational requirements related to the Investment Protection (IP) functions to be provided by the VS3 Power Supply. These functions, hereafter referred to as interlock functions, are intended to prevent damage to the VS3-PS itself and to other ITER plant systems resulting from abnormal, off-normal or fault conditions arising during any phase of operation.

Investment Protection functions are distinct from Occupational Safety and Nuclear Safety functions, which are addressed separately in sections 0 and 12. The interlock functions specified here aim at protecting equipment and plant assets by detecting hazardous situations and enforcing protective actions that limit their consequences, prevent escalation and ensure that the system is brought into a safe and recoverable state.

The operational scope of interlock functions for VS3-PS covers all phases of the system life cycle, including commissioning, normal plasma operation, degraded or fallback operation, maintenance activities, and re-energization following long shutdown periods.

This section specifies the functional role, scope and categorization of interlock functions and the principles governing their coordination and interaction with ITER central systems. Detailed technical and implementation requirements for the interlock control system are defined separately in section 7.9.5.

6.4.1 Plant Interlock System

A dedicated Plant Interlock System (PIS) shall be implemented for VS3-PS in order to coordinate all Investment Protection functions at the VS3-PS system level and to interface these functions with the ITER Central Interlock System (CIS).

From an operational perspective, the PIS constitutes the functional backbone of VS3-PS investment protection. It shall ensure that interlock functions are coherently applied across the two power converters and all shared subsystems, including common busbars, auxiliary systems and protection devices such as crowbars or fast discharge paths. For any condition requiring Investment Protection, the PIS shall enforce a transition of the VS3-PS into a defined safe state, consistent with the operating states and termination of operation requirements defined in section 6.2.3.

The detailed local fault leading to local protections or an alarm with details shall be displayed in CODAC HMI for trouble shooting. A procedure shall be provided for troubleshooting, bypass/override, confirmation of spurious triggering for local protections.

Finally, the PIS shall provide sufficient observability and diagnosability to allow operators and maintenance personnel to identify the origin and nature of interlock events, to distinguish between converter-specific and common interlock actions, and to assess the availability and status of interlock functions.

The VS3-PS conventional controllers and local controllers shall be interfaced and interlocked with the VS3-PS Plant Interlock System, using adequate communication links.

The detailed I&C architecture, hardware and networks implementing the PIS are specified in section 7.9.5.

6.4.1.1 Coordination with Central Interlock System

The PIS shall be hierarchically integrated within the ITER Plant Interlock architecture and shall interact with the Central Interlock System for the reporting of interlock events and execution feedback, as well as for the reception of plant-level interlock commands or inhibit conditions. Even where faults are locally handled by conventional control functions, their occurrence shall be reported to the CIS.

6.4.2 Interlock Functions

6.4.2.1 Purpose and functional scope

Interlock functions are deterministic protection functions whose purpose is to prevent or mitigate damage to equipment and plant systems by detecting hazardous conditions and enforcing appropriate protective actions. For VS3-PS, these functions shall protect the system against hazardous situations originating internally within the power supply, against external incoming disturbances affecting VS3-PS, and against hazardous conditions generated by VS3-PS that could affect other ITER systems.

Accordingly, interlock functions shall cover situations such as electrical overstress, thermal overload, malfunction of critical components, loss of auxiliary services, abnormal grid

conditions, induced currents or voltages from plasma events, and any uncontrolled injection of current, voltage or energy into interfaced plant systems.

The DA shall identify, define and manage the interlock functions consistent with their final design in accordance with:

1. Plant Control Design Handbook [AD46]
2. ITER Investment Protection Handbook [AD48]
3. Management of Local Interlock Functions [AD49]
4. Guidelines for the Design of the Plant Interlock System (PIS) [RD11]

6.4.2.2 Categorization and Integrity

For operational clarity and consistency with ITER investment protection practices, interlock functions for VS3-PS shall be categorized according to the protection target (VS3-PS itself or external plant systems), the origin of the hazardous situation (internal, external incoming or external outgoing), and their required integrity level.

The DA shall assign an Investment Protection Integrity Level (3IL) to each interlock function in accordance with the ITER Investment Protection Handbook [AD48] and the Management of Local Interlock Functions [AD49], based on the severity of potential damage, likelihood of occurrence, detectability and controllability of the fault, and on the results of FMECA and cost-effectiveness analyses. The integrity level of all hardware and software involved in each interlock function shall be in accordance with the assigned 3IL level of the respective interlock function.

The criteria for integrity levels and their equivalence with Quality Class and SIL are not duplicated in this specification but shall be directly referenced from the applicable ITER IP documents (see e.g. Tables 9 and 11 of [AD48]).

Whereas interlock functions with a required integrity level of 3IL-2 and above shall be implemented on Interlock-grade I&C (as per Table 11 of [AD48]), interlock functions with an integrity level of 3IL-1 may alternatively be implemented on conventional controllers, which may apply to certain internal interlock functions of VS3-PS.

6.4.2.3 Allocation and coordination

Interlock functions shall be allocated within the VS3-PS protection architecture in a manner consistent with their functional scope and required integrity. Functions protecting common components (e.g. busbars) or overall system integrity shall be implemented at the highest relevant level of the PIS, whereas functions protecting converter-specific or local components shall be implemented at the lowest level compatible with the required integrity and response time.

The level at which functions are implemented within the protection architecture shall promote the operational independence of the two power converter stages in view of the overcurrent situations resulting from power converter faults.

Where protection of external systems is involved, the corresponding interlock functions shall be coordinated with Plant or Central Interlock functions to avoid conflicting, redundant or incoherent protective actions.

For each interlock function, the triggering conditions, protective actions, reset and recovery conditions, and interaction with operating states and degraded modes shall be clearly defined and documented. The documentation shall make clear distinction between local and central actions and events.

6.4.2.4 Interlock function configuration

In addition, interlock functions shall support a controlled degree of configurability through parameters, in order to accommodate operational needs, commissioning activities, phased deployment and future evolution of the VS3-PS within the ITER programme. Such parameterisation shall not alter the fundamental protective intent of any interlock function, nor reduce the integrity level assigned to it.

The management of interlock-related parameters shall be governed by ITER Central Interlock System (CIS) policies. In particular, parameters affecting interlock behaviour (such as thresholds, enable/disable conditions, masking under authorised states, or timing constraints) shall be configurable only through mechanisms approved and supervised by CIS, ensuring traceability, access control, versioning and consistency at plant level. A preliminary guideline for the configuration of investment protection and protection related systems is provided in [RD14].

Local or conventional control systems shall not be allowed to modify interlock parameters autonomously, except where explicitly authorised within the CIS governance framework. The VS3-PS design shall therefore ensure that any operational flexibility introduced through parameterisation remains fully compatible with the overall ITER investment protection strategy and does not compromise plant-wide coherence of interlock functions.

6.4.2.5 Actuators

Any single or combination of actuator(s) or actuation mechanism(s) involved in an interlock action shall have an integrity level in agreement with the integrity classification of the respective interlock function. This applies for dedicated actuators (such as the crowbar system) and for components and mechanisms already part of the power supply (such as gate drive disables).

The crowbar system may be considered as an actuator for the final protection layer; however it is expected that there are many investment protection events and actions that do not have to escalate to this final layer.

6.4.3   Minimum Set of Interlock Functions

Below is a list of functions that are known from a transversal high-level analysis of the system's functions in the context of the ITER tokamak.

There might be more interlock functions or less interlock functions dependent on the final design of the VS3 power supply. For instance, if the design presents something as intrinsically investment-safe - fewer interlock functions might be needed.

The designer shall carry on the failure mode analysis into the details of the design they will propose. The list below is to be extended with all interlock functions resulting from the identification and definition of interlock functions as provided for in section 6.4.2.

6.4.3.1 CIS stop command

The VS3 Power Supply System shall implement a function that terminates the operation of the power supply immediately upon receipt of the corresponding command from CIS. The power supply output shall be disabled within 1 ms after receipt of such command and the DC Link shall be de-energized.

A stop command may be issued by CIS in case of lack of cooling water flow in the VS coils, for example.

The integrity level of this function shall be at least 3IL-3.

6.4.3.2 *Power permit signal*

The VS3 Power Supply System shall implement a power permit signal that inhibits the energization of the output circuit out-of-pulse for all circuit configurations in which the power supply is connected to the VS coils (i.e. and not the dummy load).

The integrity level of this function shall be at least 3IL-3.

6.4.3.3 *Overcurrent Protection – Power Supply*

The VS3 Power Supply System shall implement short-circuit and overcurrent protection(s), for all relevant power supply components and parts that need active protection thereagainst. The identification and implementation of these functions shall be based on the FMECA and industry's best practices.

Passive overcurrent protections, such as fuses, current limiting devices, etc., are in principle not considered part of the Overcurrent Protection interlock functions, nevertheless their status shall be reported to CIS and the appropriate actions to safeguard the power supply system shall be taken by the local Plant Interlock Controller.

6.4.3.4 *Overcurrent Protection – VS3 Coil Circuit*

The VS3 Power Supply System shall limit the current in the VS3 coil circuit to a maximum magnitude of 90 kA under all probable circumstances, through the implementation of short-circuit and overcurrent protection function(s).

In particular, this protection shall protect the coil circuit against power supply fault currents, by triggering the crowbar system.

The instantaneous trip threshold of the short-circuit protection shall be defined such that spurious tripping during normal operation is avoided, yet such that the instantaneous current in the coil circuit during short-circuit events does not exceed the stated 90 kA. The instantaneous trip threshold shall not be less than 83 kA.

The limit of 90 kA applies to both the 6-turn and 8-turn configuration and relates to the lowest limit in the coil circuit.

An Inverse Time Overcurrent protection shall be implemented in accordance with IEC 60255-151 / ANSI 51 or similar. This is currently only a provision, no inverse time overcurrent protection limit is foreseen for the coil circuit. Therefore, all parameters associated to the inverse time overcurrent protection shall be programmable.

Table 6-7: Overcurrent Protection levels for VS3 Coil Circuit

VS3 Coil Circuit Overcurrent Protection	Level	Remarks
Maximum admissible current	**90 kA**	Both polarities, includes any overshoot
Instantaneous trip level	≥ 83 kA	To be defined by DA
Inverse time overcurrent trip level	-	Conform ANSI 51 or similar

The integrity level of the overcurrent function shall be at least 3IL-3.

6.4.3.5 Overvoltage Protection

The VS3 Power Supply System shall implement overvoltage protection(s) for all relevant power supply components and parts that need active protection against transient and static overvoltage conditions. The identification and implementation of these functions shall be based on the FMECA and industry's best practices.

Among others, this protection is to protect both the power supply against (induced) overvoltage from the coil circuit, and the coil circuit from erroneous overvoltage generated by the power supply.

As a minimum, the components and subsystems listed Table 6-8 shall be actively protected against overvoltage. The subsequent action(s) shall be defined by DA; suggestions for possible actions are included in Table 6-8.

The voltage protection limits shall be defined such that no permanent or significant service life reducing damage is sustained during such overvoltage events.

Table 6-8: Overvoltage Protection - minimum set of components and subsystems

Component / Subsystem	Possible action(s)	Remarks
DC Link & Capacitor Bank	Fast discharge & stop inverter/rectifier	
VS3 coil circuit	Shunt with crowbar and/or clamp to DC Link	Reference node: VS3-PS output terminals
AC input side	Isolation through Circuit Breaker	

Passive overvoltage protections, such as Break-Over Diode implementations in the crowbar, are in principle not considered part of the Overvoltage Protection interlock functions, nevertheless their status shall be reported to CIS.

Hence the state of conductance of each device providing passive overvoltage protection (e.g. varistor, BOD, thyristor, bypass switch, etc.) shall be monitored and in case of activation, the power supply shall transition to the appropriate safe state by the PIS and the status of the interlock function shall be communicated as active to CIS.

6.4.3.6 Overtemperature Protection

The VS3 Power Supply System shall implement overtemperature protection(s) for all critical power supply components and parts that need active protection against overheating. The identification and implementation of these functions shall be based on the FMECA and industry's best practices.

As a minimum, the temperature of the following subsystems and/or key components thereof shall be monitored, and active protection shall be provided:
  - Semiconductor switch devices/modules of inverters and rectifiers
  - Crowbars
  - Fast discharge units

- Pre-charge system
- Dummy load

The number and specific location of sensors is to be defined by DA in accordance with the FMECA. Furthermore, the DA shall determine and list the appropriate alarm and trip temperature levels for each component and associated temperature measurement(s).

6.4.3.7 Busbar Overtemperature Protection

The VS3 Power Supply System shall implement overtemperature protection for the VS3 IVC Busbars and VS3 Extension Busbars in accordance with the requirements in section 9.6.

The protection shall comprise alarm and trip thresholds, with the corresponding actions as defined in Table 6-9. The logic for alarms and tripping shall be individually applied to all instrumented busbar segments.

It is to be noted that in the absence of cooling water flow, the temperature reading may not reflect the actual temperature of the affected busbar segment(s). Nonetheless, in the absence of cooling water flow, the busbars can sustain the VS3 nominal operating current without overheating for a limited amount of time [RD53]. Therefore, in case of contradictory measurements of flow and temperature, a delayed shutdown is permitted to reduce spurious tripping. The duration of this delay shall be programmable and will be confirmed by IO in due course.

Table 6-9: Busbar Overtemperature Protection – logic for alarms and tripping

Flow switch	Temperature sensor	Action	Remarks
OK	$T \leq T_{alarm}$	No action	
OK	$T \geq T_{alarm}$	Alarm, followed by power supply trip after predefined duration	
OK	$T \geq T_{trip}$	Trip	
NOK	$T \leq T_{alarm}$	Alarm, followed by power supply trip after predefined duration	
NOK	$T \geq T_{alarm}$	Trip	
NOK	$T \geq T_{trip}$	Trip	

The integrity level of the busbar overtemperature function shall be at least 3IL-2.

6.4.3.8 Insulation / Earth Fault Protection

The VS3 Power Supply System shall implement protection(s) against earth and insulation faults.

The operation of the VS3 Power Supply shall be stopped instantly upon the occurrence of the first insulation or earth fault.

The correct and early detection of earth-fault conditions, followed by the immediate termination of power supply operation upon the first occurrence of an earth fault, is essential for the protection of the VS coils and for preventing larger damage.

6.4.3.9   Transformer Protection

The VS3 Power Supply System shall implement at least the following interlock functions (or equivalent) for the protection of each individual power transformer:

- ANSI 49T or ANSI 49RMS: Overtemperature
- ANSI 87T: Differential protection
- ANSI 50: Short circuit protection
- ANSI 59N: Ground fault protection
- ANSI 67: Directional earth fault

The interlock functions shall be implemented using commercial protection relays, which shall be directly interfaced with the MV circuit breakers using a hardwired connection. The status of the implemented protections shall be communicated to CIS, irrespective of commercial protection relays being used.

6.4.3.10 Capacitor Bank Protection

The VS3 Power Supply System shall implement all necessary protections for ensuring the integrity of the Energy Storage Capacitor Bank. The identification and implementation of these functions shall be based on the FMECA and industry's best practices.

As a minimum, the following scenarios shall be covered by this protection:

- Loss of capacitor bank, e.g. due to tripping of main fuse
- Sudden reduction in State-of-Health (SoH), e.g. due to tripping of cell fuse(s)

6.4.3.11 Uncontrolled Rectifier Mode

The VS3 Power Supply System shall implement protection(s) against uncontrolled operating modes of the rectifier stage, including but not limited those caused by insufficient DC Link voltage in consideration of the rectifier's anti-parallel diodes.

The identification and implementation of these function(s) shall be based on the FMECA and industry's best practices.

Where possible, these protections shall be implemented using COTS components.

6.4.3.12 Component and System Interlocks

The VS3 Power Supply System shall implement all necessary protection functions to detect, avoid and mitigate dangerous system configurations that could damage the power supply during operation or during any component malfunctioning. The dangerous configurations shall be identified and defined as part of the FMECA. The subsequent identification and implementation of the required protection functions shall be based on this FMECA along with industry's best practices.

As a minimum, the following dangerous configurations and scenarios shall be covered by this protection:

- Inadvertent actuation / operation of controls
- Contradicting control actions on disconnector and earthing switches
- Operation while one of the power converters is non-operational
- Operation while any of the VS3-PS subsystems or components is non-operational
- Operation of non-load-switching (electro)mechanical switches under non-zero current

- Operation on dummy load while load circuit is connected
- Crowbar operation while inverter stage is operational
- Fast discharge system conductive while rectifier stage is operational
- Pre-charge circuitry active while Active Front-End is operational
- Discharge of coil circuit excess energy without sufficient voltage margin on DC Link
- Loss of services (including but not limited to those described in section 6.8)

6.4.3.13 I&C System Integrity

The VS3 Power Supply System shall monitor the status of its I&C System, including all communication channels part thereof, and implement protections to take the necessary actions in case the integrity of the system does not allow the robust operation of the power supply. The identification of the relevant I&C components and communication channels, as well as the implementation of the protection functions shall be based on the FMECA and industry's best practices.

6.4.4 Failure Modes, Effects and Criticality Analysis (FMECA)

The DA shall perform Failure Modes, Effects and Criticality Analysis (FMECA), covering all the permanent components in the scope of this technical specification. Further details on the process in relation to the RAMI requirements are provided in section 6.5.

6.4.4.1 Fault Matrix

The DA shall develop and maintain a fault matrix, which shall contain the exhaustive list of signals, conditions and events that lead to interlock action(s).

For each protection function, the fault matrix shall unambiguously describe which inputs are considered, what logic is applied, and what actions are taken.

In the final version of said matrix, each line shall correspond to a signal/event/condition and include the associated sensor reference, controller name and terminal block reference.

The fault matrix will be used as the basis for interlock control design and functional tests during FAT, SAT, commissioning and troubleshooting during operation.

6.5 Reliability, Availability, Maintainability & Inspectability (RAMI)

The DA shall incorporate the ITER RAMI Programme [AD10] and all associated requirements in the design and design process of VS3-PS.

The VS3-PS system shall comply with the availability requirements defined in Table 6-10

Table 6-10: availability requirements for the VS3-PS System

Main function	Availability

To produce and supply appropriate power to the VS coils	99.4%
To ensure proper grounding of the coils	99.4%
To provide measurements to PCS	99.9%

The reliability characteristics shall be demonstrated in accordance with the ITER RAMI Programme [AD10].

The maintainability characteristics shall be demonstrated by the DA, as part of the qualification process.

It shall be noted that the RAMI requirements are defined by SRD-41 [AD4], in turn propagated from the ITER Project Requirements [AD3]. However, the reliability requirements from the point of view of investment protection, i.e. avoiding loss or damage of equipment, might result in different reliability requirements.

6.5.1   General

It is required that the DA demonstrates that its design meets the RAMI requirements defined in the PRs.

As a first step, the Preliminary Design Review shall include presentation/demonstration/de of a completed RAMI analysis, on the basis of the functional breakdown and first analysis performed by IO, with availability & reliability estimates (RBDs), and definition of the technical risks & associated mitigation actions to be implemented (FMECA).

In a second step, the Final Design Review shall demonstrate how those mitigation actions have been implemented to reach the targets, refer to:
1. ITER RAMI Programme [AD10] as a methodology,
2. Template for RAMI Analysis Summary Reports [RD17] as template to be followed, and
3. Working Instruction for Reliability, Availability, Maintainability and Inspectability (RAMI) Analysis [AD11] which defines the process itself.

Each revision of the RAMI analysis summary report shall begin with a kick-off meeting with system Responsible Officer (RO) and RAMI RO, the RAMI process, applicable methodology, data sources and tools shall be described by RAMI RO. The system RO and RAMI RO shall confirm the target availability value from Project Requirements or other applicable documents, define the inputs for the system functional analysis, list the major constraints related to the systems Inspectability and Maintainability (access rules, time required to access the components, safety considerations that shall be considered while calculating the time required to access and repair).

6.5.2   RAMI Objectives

The VS3 Power Supply System shall be designed for a 20 years' operating life (refer to Table 6-4) under the necessary and appropriate maintenance.

The inherent reliability, availability, maintainability & inspectability objectives of the components under the DA's control shall be defined within the RAMI Analysis submitted at PDR & FDR so that the availability of the main functions of the system is consistent with the RAMI targets defined in the Project Requirements.

The DA shall demonstrate that the proposed design solution has acknowledged the results of the RAMI analysis with regard in particular to maintenance, availability of spares (include the logistical availability of spares).

6.5.2.1 Reliability

The DA shall respect the reliability targets highlighted in the RAMI analysis.

6.5.2.2 Inspectability

Inspectability objective shall be defined within the RAMI Analysis.

6.5.2.3 Maintainability

When standard IO catalogue hardware items are employed, the maintainability is considered as fulfilled.

Software shall be maintainable by using the source code with the standard ITER software development toolchain to produce the software artifacts used. In case a non-ITER toolchain is used or the source code is IP protected, the maintainability shall be demonstrated.

6.5.3 Test and Validation of RAMI Performance

Reliability characteristics shall be demonstrated by the DA as part of the VS3 Power Supply qualification process.

On the basis of the first RAMI analysis, the DA shall prepare Reliability Block Diagrams (RBDs) and a Failure Modes, Effects and Criticality Analysis (FMECA). It shall incorporate the description of faults and their causes and consequences, the failure rate, test periods, repair times and consequences of failure, which are dependent on the configuration of the installation, and the risk-mitigation actions associated. These are to be presented by DA at Preliminary Design Review stage. During the Final Design Review, the implementation of the risk-mitigation actions shall be demonstrated.

These demonstrations shall ensure accuracy of elapsed times and efficiency of support equipment needed for task performance.

6.5.4 RAMI Risk Mitigation in the Design

Actions shall be taken to mitigate the risks in various project phases (design, test, operation and maintenance) in order to lower the criticality of function failures.

Relevant applicable documents for the RAMI analysis include but are not limited to:

- Template for RAMI Analysis Summary Reports [RD17]
- RAMI Analysis How-To Guidance [RD16]
- ITER Concept of Operations [RD19]
- ITER Operational States [AD47]

Reliability calculations and availability calculations shall be taken into account before acceptance of any new design.

The risk-mitigation actions are to be presented by the DA at Preliminary Design Review and implemented for the Final Design Review stage.

6.5.5 Maintenance and Spares

The DA's design shall recognise the impact of the availability of space to undertake the required maintenance & the effects this will have on the period for the maintenance following ITER RAMI Analysis Program [AD10].

RAMI results shall be taken as a prime consideration in the defining of the list of critical spares.

When considering the spare parts critical list, the space available to install the parts shall also be considered as a major factor in what is a critical part. That is to say that if due to limited space or the need to remove other components to install another component then this should be highlighted in the list as a critical part.

The DA shall provide a list of spare parts that are to be stocked on site.

A list of the proposed spare parts shall be submitted to IO with the Final Design Review (FDR) and shall be based on the following factors:

- Inherent reliability of equipment components (i.e. mean time between failure (MTBF, MTTR, etc.)
- Criticality of equipment components
- Response and coverage of planned maintenance
- Availability of parts on or near the ITER site
- Replacement parts replenishment/repair time
- Technical skills required to diagnose and resolve failures
- Risk of spares obsolescence
- Available space

Final decision on spares provisioning will be made by IO.

To avoid inventory increase, the DA shall use as much as possible components defined as project standards in ITER Standard Component Register (ITER_D_35UVAQ), and otherwise makes maximum use of Commercial Off The Shelf (COTS) equipment and components.

The DA shall inform IO of any risk regarding components' obsolescence and make all pertinent recommendations to eliminate that risk.

6.6 Power Supply Electrical Load

6.6.1 Electrical load impedance

The VS3 Power Supply shall be designed for operation with the specified performance requirements (current levels, dynamics, etc.) on the electrical load impedance comprised of the VS3 coil circuit with either 6-turn or 8-turn VS-coil configuration.

The performance of the power supply (output levels, dynamics, stability, voltage/current ripple, etc.) shall be assessed taking into account the electrical load impedance as described here below, including but not limited to the complex impedance of Figure 6-6.

The transition between both configurations is only required in static conditions when the VS3-PS is in OFF state (de-energized).

The electrical load impedance of the VS3 Power Supply is comprised of:
- the VS-coil turns of PBS 15.IV,
- the VS-coil feeders and feedthroughs of PBS 15.IV,
- the VS3-related IVC busbars of PBS 41.V3.BB
- the VS3 Linkboard of PBS 41.V3.BB
- the VS3 Extension Busbars of PBS 41.V3.BE

The computed impedance of the VS-coil and feeders is presented in section 9.2.3.

The load impedance comprising all above components is provided in [RD46] for 8-turn and 6-turn VS-coil configuration, on the basis of the analysis reports on the IVC impedance [RD44], [RD45].

The anticipated total resistance and total inductance as computed in [RD46] are given in Figure 9-2.
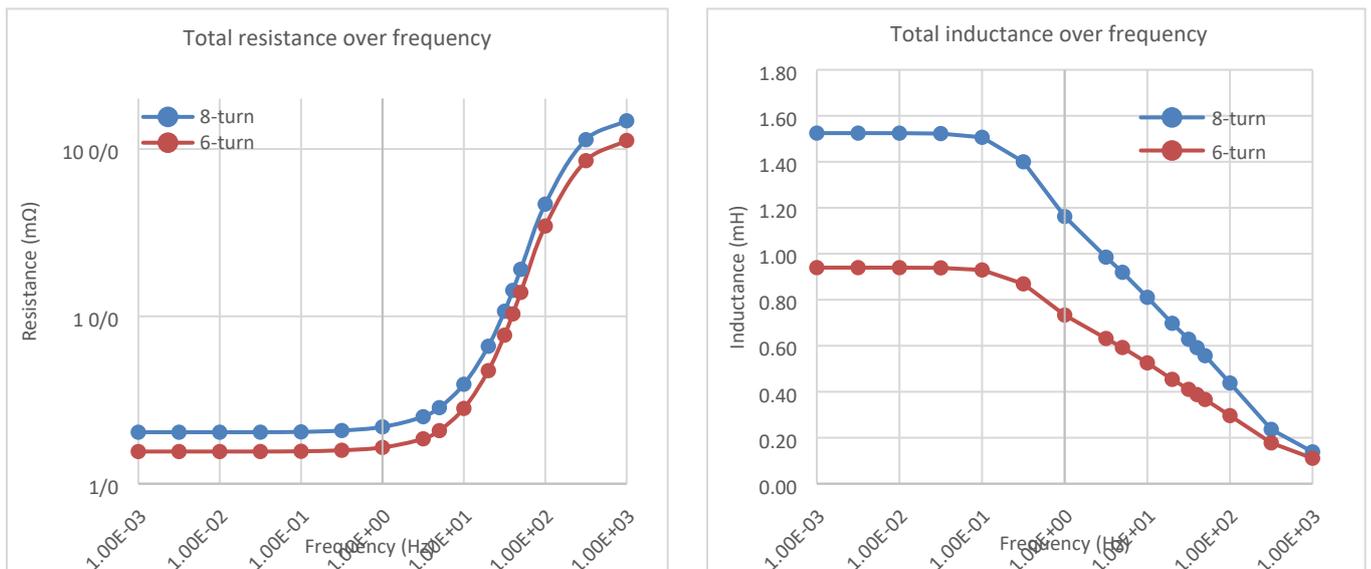
Figure 6-6: anticipated power supply load impedance for 8-turn and 6-turn configuration. Obtained from [RD46].

The analyses reported in [RD44], [RD45] and [RD46] list several limitations that potentially affect the accuracy of the computed load impedance, particularly at frequencies above 50 Hz. Such limitations include simplifications in the finite element model, e.g. omittance of blanket modules, cryostat, TF coils, TF casing and plates, the feedthroughs, the design details of IVC components, etc. For feeders and busbar segments, the impedance is computed based on the linear length and the unitary impedance of the segments, thereby omitting e.g. bends and conductor geometries in accessories like connection boxes.

In addition, the presented circuit resistance and inductance correspond to an Equivalent Series Inductance (ESL) model, in which and capacitance has been omitted. Indeed, the aforementioned impedance reports do not consider stray capacitance, predominantly formed by the conductor-to-case capacitance of the busbars, feeders and coil.

This stray capacitance shall be included by DA in the analysis and documentation used for design justification, e.g. on EMI and fault currents.

6.6.2   Electrical load variations

6.6.2.1   Nominal load impedance uncertainty

In order to accommodate any possible variation and uncertainty in the nominal load impedance, the DA shall apply the following margins, both positively and negatively, for the design of VS3-PS:

Nominal load impedance margins
-    Up to 100 Hz: ±10%
-    Above 100 Hz: ±25%

The margins shall be applied on both the resistive and inductive part of the impedance, in any combination.

6.6.2.2   Reconfiguration of coil-turns

The VS3 Power Supply shall be capable of accommodating changes in the load impedance due to the reconfiguration of coil-turns (change from 6-turn to 8-turn configuration and vice versa), while maintaining its full performance characteristics. The reconfiguration occurs only when the power supply is shut down and deenergized.

Should the VS3-PS not be capable of delivering the performance requirements set out in sections 6.1 and 6.2 for both the 6-turn and the 8-turn configurations under a single set of control parameters, then the VS3-PS shall be capable of setting its control parameters according to the actual coil turn configuration.

6.6.2.3   Dynamic changes to the electrical load impedance

The VS3 Power Supply shall be capable of accommodating dynamic changes of up to 10% in the load impedance, i.e. during operation of the power supply, due to e.g. temperature changs, varying plasma position, coupled electromagnetic effects, etc.

The output regulation controller of VS3-PS shall be designed to allow such variations without any real-time manual tuning and while maintain the output performance.

6.6.2.4   Short-Circuit Requirements

The VS3 Power Supply output shall be short-circuit proof, i.e. no damage to VS3-PS or the VS3 coil circuit shall result from a (sudden) short-circuit condition, including but not limited to bolted short-circuits, arcing, dielectric breakdown, etc.

In case of (sudden) low load impedance, the power supply protections described in sections 6.4 and 6.7 shall ensure that the power converter's design values are not exceeded.

6.6.2.5 Operating under no-load

Operating under no-load shall be possible without causing damage to the power supply and the busbars.

6.6.3 Induced voltage and current

The VS3 Power Supply shall be designed and controlled to withstand the induced voltage and current in the VS3 coil circuit, caused by e.g. VDEs, plasma disruptions and transients in the superconducting CS, PF, TF, CC coils due to e.g. fast discharges.

Provisions and/or operational procedures shall be provided to withstand such induced current and voltage events even when the power supply is not operational.

6.6.3.1 Induced current

The induced current has been calculated in [RD47] for several scenarios and for a strongly simplified power supply circuit. As opposed to earlier work, which has computed the induced current due to transient plasma events as sole event, this study considers the VS3 control action prior and during such event to calculate the combined maximum current in the VS3 circuit.

Three control actions are considered, summarised as follows:

1. Reference: no control action is applied to the VS3 system, i.e. only the plasma transient
2. Control: a 60kA impulse is fired signed to generate a restoring force on the plasma
3. Error: a 60kA impulse is fired signed to generate a destabilising force on the plasma

Figure 6-7 shows the computed maximum currents in the VS3 circuit for 12 different plasma events and for the 8-turn VS-coil configuration. The maximum current magnitude in the VS3 coil circuit for the investigated control actions and scenarios is 86 kA. This is higher than the induced current for the transient plasma event alone, with a maximum of around 55 kA, yet considerably lower than the simple linear combination of the control action currents and induced currents due to transient plasma events.
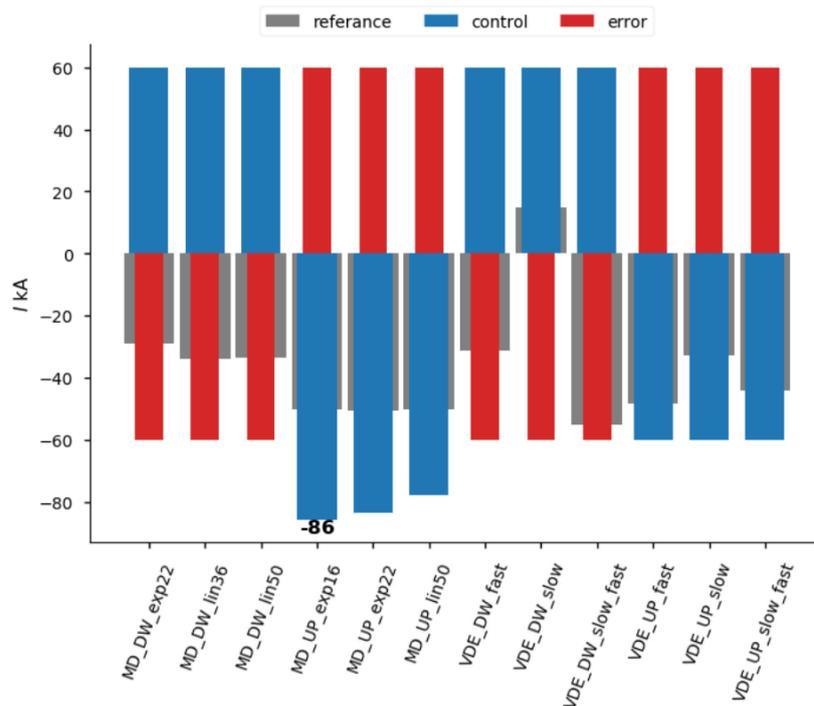
Figure 6-7: maximum VS3 currents including a 60 kA control impulse (spiked control profile) commuted for 12 transient plasma events and for 8-turn configuration. Adopted from [RD47].

Similar analyses have been performed for the 6-turn configuration, for which it was found that the maximum current magnitude in the VS3 circuit is increased by approximately 12% to 95.4 kA. Table 6-11 summarizes the results for the worst-case inputs.

Table 6-11: summary of worst-case input for 6-turn operation (single turn removed from upper and lower VS coils). Data adopted from [RD47].

Sub-system	Transient event	Time t	Current I
Upper VS coil	MD_UP_exp16	25.0 ms	-94.8 kA
	VDE_UP_slow_fast	910.2 ms	-44.3 kA
Lower VS coil	MD_DW_exp22	220.0 ms	80.0 kA
	VDE_DW_slow_fast	290 ms	80.0 kA
VS coils + feeders	MD_UP_exp16	27.2 ms	-95.4 kA

The VS3 Power Supply shall be designed and controlled to withstand all possible induced currents in the VS3 coil circuit, with as a minimum 95.4 kA and 86 kA for the 6-turn and 8-turn configuration, respectively. A margin of at least 20% on top of any calculated induced current shall be included. For the duration of such events, a minimum of 100 ms shall be assumed.

To protect the power supply, the VS3-PS output shall be shunted instantly through the crowbar once the current in the VS3 coil circuit, under the influence of induced voltages, exceeds the design ratings of the power converters.

6.6.3.2 Induced voltage

In open-circuit or high output impedance conditions, the induced voltage may exceed the rated voltage of VS3-PS. Provisions shall therefore be included to ensure that the design ratings of the power supply are not exceeded during such events, which may comprise shunting the coil circuit through the crowbar or clamping the output voltage to the DC Link.

6.7 Conventional Power Supply Control Features

The VS3 Power Supply shall implement conventional power supply control features that allow limiting and tripping the output in case programmable limits are exceeded.

The aforementioned control features shall be implemented on conventional controllers, not part of the interlock system. Their purpose is to provide additional functionality to the power supply user, for instance to allow for progressive commissioning with increasing voltage/current, and not necessarily to provide investment protection functions.

All Conventional Power Supply Control Features, including but not limited to the features listed in below subsections, shall be capable of being enabled/disabled via the interface with ITER's Central I&C System.

6.7.1 Overcurrent Limiting and Overvoltage Limiting

The VS3 Power Supply shall implement Overcurrent Limiting (OCL) and Overvoltage Limiting (OVL) functions, which actively limit the power supply output to the defined limits.

The limits taken into account for this function shall comprise both predefined (internal) limits (e.g. design limits) and user-programmable limits. The user-programmable limits shall be made available for reading and writing through the interface with ITER's Central I&C system; the predefined limits shall only be available for reading through said interface.

The power supply's output regulation controller shall actively limit the VS3 coil circuit voltage and current to the defined limits, both for inputs (setpoints) exceeding the limits and for transient events in the load circuit, due to e.g. plasma disruptions, within the limits of power supply's rated voltage and current.

6.7.2 Overcurrent Tripping and Overvoltage Tripping

The VS3 Power Supply shall implement Overcurrent Tripping (OCT) and Overvoltage Tripping (OVT) functions, which instantly trip the power supply output in case the defined trip levels are exceeded.

The trip values taken into account for this function shall comprise both predefined (internal) values (e.g. absolute design limits) and user-programmable values. The user-programmable trip levels shall be made available for reading and writing through the interface with ITER's Central I&C system; the predefined trip values shall only be available for reading through said interface.

The power supply's output stage shall instantly be tripped in case the trip levels are exceeded. The power supply shall remain in the operational state, the DC Link shall remain energized, only the output stage shall be disabled. A "tripped" sub-state part of the operational state may be foreseen for this purpose.

Selectivity between the Tripping and Limiting functions through the definition of the respective trip and limit levels shall be assured, i.e. when the limit level is programmed below the trip level then the output shall be limited and not tripped.

Selectivity between the conventional Tripping and Limiting control features and the (investment) protection functions shall be assured for:
- any current limit/trip level up to 80% of the rated power supply current
- any voltage limit/trip level up to 50% of the rated power supply voltage

6.7.3 Overtemperature Limiting

The VS3 Power Supply shall implement an Overtemperature Limiting (OTL) function, which limits the output voltage, current and/or power when the thermal margins are significantly reducing and an overtemperature condition is imminent.

The need for this function arises from the pulsed operating nature and the specific duty cycle requirements, whereas no strict limits are being applied on the input (setpoint) side of the power supply, meaning any number of pulses may be requested.

This function is intended to avoid tripping the power supply due to overtemperature conditions, allowing the operation at lower currents (e.g. for continuous noise operation) to continue, while thermally recovering from the pulsed operation.

The OTL function shall not be necessary nor be activated for any normal operating condition and mission profile as specified in section 6.1 - Performance requirements.

The VS3 Power Supply shall report the status of activation of the Overtemperature Limiting, i.e. when limits are applied to the output, irrespective whether those limits are already activity limiting the output for the given input setpoints or not.

6.7.4 Output Regulation Status Reporting

The VS3 Power Supply shall continuously monitor and report its output regulation status through a dedicated "Out-of-Regulation" signal as follows.

The update rate of this signal shall not be less than 1 kHz.

6.7.4.1 Out-of-Regulation

The Out-of-Regulation (OoR) signal is to be asserted when the power supply is not able to produce the requested voltage or current at the output.

Causes for such condition include but are not limited to:
- In closed-loop voltage control mode:
  o The voltage setpoint exceeds the Overvoltage Limit value
  o The current required to produce the requested voltage setpoint (static) exceeds the Overcurrent Limit value

o The current required to produce the requested voltage waveform slew-rate (dynamic) exceeds the Overcurrent Limit value

- In <u>closed-loop current control</u> mode:
    o The current setpoint exceeds the Overcurrent Limit value
    o The voltage required to produce the requested current setpoint exceeds the Overvoltage Limit value
    o The voltage required to produce the requested current waveform slew-rate (dynamic) exceeds the Overvoltage Limit value

6.8 Abnormal operating scenarios

The operation and actions of the VS3 Power Supply under abnormal conditions, such as in case of loss of services, loss of communication, etc., shall be addressed and defined as part of the FMECA (section 6.5) and implemented as interlock functions where required. Nevertheless, the following specific requirements shall be taken into account.

6.8.1 Loss of services

6.8.1.1 Internal protection requirement

The VS3 Power Supply shall monitor the conditions of all relevant interfaced services (SSEN, PPEN, CCWS, etc) and, in case of loss or degradation of such services, transition into a safe state and raise the necessary alarms and interlock events to ITER Central I&C System in accordance with [R247] of PCDH [AD46]. No damage or subsequent inoperativeness shall be resulting from such event.

6.8.1.2 Loss of CCWS

The VS3 Power Supply shall monitor the flow and temperature of the incoming cooling water.

In case of absence of flow or elevated water inlet temperatures, the VS3-PS shall perform a controlled shutdown under the provisions of section 6.2.3. All I&C functions shall remain operational.

Should the design margins permit, continued operation for several seconds after issuance of the respective alarm and before terminating the VS3-PS operation would be desirable for gradually terminating the plasma operation. The duration during which VS3-PS may continue to operate (at full performance) would then need to be carefully defined.

6.8.1.3 Loss of HVAC

A direct interface with the HVAC or Building Management System is not foreseen. Consequently, the loss of HVAC is to be detected using dedicated ambient temperature sensors at all necessary locations, or handled via the regular overtemperature protections (section 6.4.3.6). I&C functions shall remain operational to within the thermal limits of their hardware.

Should the design margins permit, continued operation for several seconds after issuance of the respective alarm and before terminating the VS3-PS operation would be desirable for gradually terminating the plasma operation. The duration during which VS3-PS may continue to operate (at full performance) would then need to be carefully defined.

6.8.1.4 Loss of PPEN

The VS3 Power Supply shall monitor the status (e.g. voltage, frequency) of its 22 kV supply. In case of voltage and/or frequency levels outside of the design values, including absence of supply, the VS3-PS shall perform a controlled shutdown under the provisions of section 6.2.3. All I&C functions shall remain operational.

Continued operation using the energy remaining in the ESCB for several seconds after issuance of the respective alarm and before terminating the VS3-PS operation would be desirable for gradually terminating the plasma operation. The duration during which VS3-PS may continue to operate (at full performance) would then need to be carefully defined.

6.8.1.5 Loss of SSEN – Class IV

The VS3 Power Supply shall monitor the status (e.g. voltage, frequency) of its LV Class IV supply. In case of voltage and/or frequency levels outside of the design values, including absence of supply, the VS3-PS shall perform a controlled shutdown under the provisions of section 6.2.3. All I&C functions shall remain operational.

In case of loss of adequate Class IV LV supply, continued operation for several seconds after issuance of the respective alarm and before terminating the VS3-PS operation would be desirable for gradually terminating the plasma operation. The duration during which VS3-PS may continue to operate (at full performance) would then need to be carefully defined.

6.8.1.6 Loss of SSEN – Class II-IP

In case of loss of SSEN Class II-IP power, the VS3-PS shall autonomously transition into a safe, deenergized state while issuing the relevant alarms/events to ITER Central I&C System (e.g. through anticipation by brownout protection).

6.8.2 Loss of communication

The VS3 Power Supply shall monitor the conditions of all relevant internal and external (i.e. CODAC/CIS/PCS) communication channels, in case of loss or degradation of such channel(s), transition into a safe state and raise the necessary alarms and interlock events to ITER Central I&C System. No damage or subsequent inoperability shall result from such an event.

7 Subsystem Technical Requirements

7.1 Architecture and arrangement

The VS3 Power Supply shall comprise two physically and operationally independent power converters in push-pull configuration, connected to the 4-terminal VS3 coil circuit, in accordance with the Single Line Diagram of [RD50].

A strongly simplified, high-level and non-contractual diagram is provided in Figure 7-1.
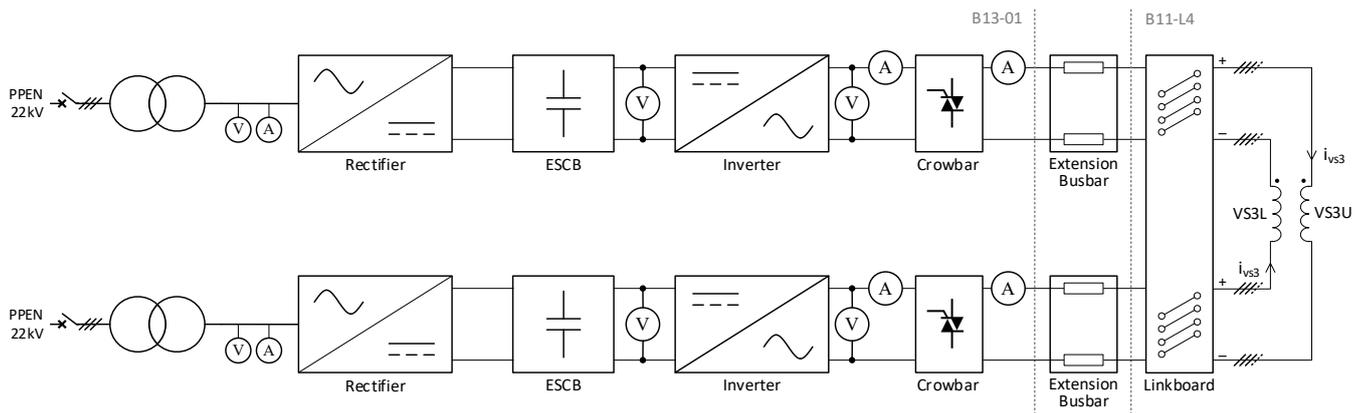
Figure 7-1: simplified diagram showing main architecture of VS3-PS

The two power converters shall be physically and functionally independent, as much as reasonably possible, for the purpose of modularity and minimizing common-mode failures that could lead to significant fault currents in the coil circuit.

Irrespective of their physical and operational independence, the two power converters shall always be operated in unison, i.e. the VS3 Power Supply shall only be operational in case both power converters are operational. This applies to both conventional control and protections.

Similarly, the two crowbar units constituting the crowbar system shall be operated in unison at all times, with the sole exception of any passive overvoltage protections.

7.1.1 Converter breakdown definitions

For the purposes of the following sections, the definitions governing the hierarchical breakdown of the rectifiers and inverters into modules and switches, as described below and illustrated in Figure 7-2 shall apply.

The rectifier/inverter of each power converter is comprised of one or multiple rectifier/inverter modules. The modules are typically connected in parallel through an inductor for current-balancing purposes and may operate at different switching phases (interleaved operation).

Each rectifier/inverter module is subsequently composed of one or multiple switch modules. When discrete semiconductors are employed, the switch module is composed of discrete switches arranged in bridge configuration. When multiple semiconductor switches are integrated within a single physical module, the switch module is comprised of one or several leg- or bridge-modules.
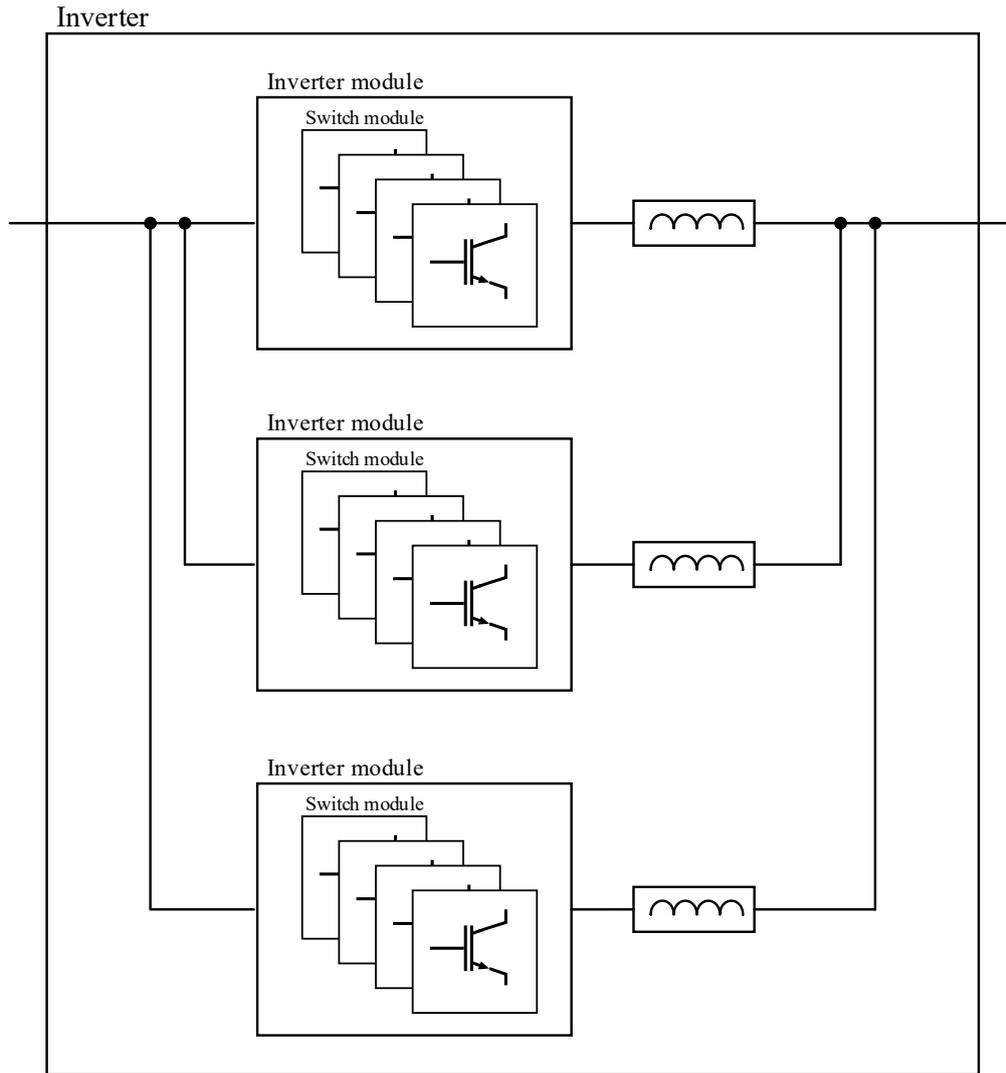
Figure 7-2: breakdown definitions of inverter into inverter and switch modules, and same for rectifier

7.2 Rectifier Stage

This section covers the specific technical requirements for the rectifier stage of each power converter. The rectifier stage is defined as all components between the 22kV switchgear and the DC Link, comprising the step-down transformer, ac/dc rectifier and all related auxiliary components.

7.2.1 General requirements

7.2.1.1 Topology & technology

The rectifier stage of each VS3-PS power converter shall comprise an Active Front-End rectifier, i.e. be based on Voltage Source Converter (VSC) technology.

7.2.1.2 Inrush current

The appropriate mechanisms shall be implemented to limit the inrush currents of the rectifier stage, such as those caused by transformer magnetization and initial charging of the DC Link capacitance, to the maximum levels imposed by the PPEN (refer to section 9.7.3).

Sequential starting of the power converters may be considered for reducing inrush currents.

The maximum allowable inrush current shall further be coordinated with the setting of the protections in the 22kV substation of ELM-PS.

7.2.1.3 Uncontrolled rectification

All necessary sensors and mechanisms shall be included to detect, avoid and where needed appropriately terminate the uncontrolled conduction of the rectifier stage, outside of the pre-charging operation, for instance in the event of a sudden drop of DC Link voltage.

7.2.1.4 Overvoltage protection

The necessary overvoltage protection devices shall be implemented on the AC side to protect the transformer and downstream equipment against possible voltage surges on the 22 kV network, in accordance with applicable standards and standard industry practices.

7.2.1.5 Disconnector switch

A disconnector switch at the secondary (LV) side of the transformer shall be implemented for local isolation from the AC supply.

7.2.2 Step-down transformer

Step-down transformer(s) shall be implemented to step down the voltage and to provide galvanic isolation between the PPEN and each power converter, in accordance with the relevant standards.

The transformer shall be designed and tested in accordance with IEC 60076-11 [CS1].

7.2.2.1 Transformer type

The transformer shall be of the cast resin dry-type. Oil-filled transformers are not acceptable; refer to section 8.3.2.

7.2.2.2 Secondary winding voltage

The secondary-winding voltage shall be defined by DA taking into account, among other factors, efficiency considerations, commercial availability, and the extent of non-utilized ESCB gross energy storage.

7.2.2.3 Rating

The transformer shall be dimensioned for the continuous and pulsed operating duties of VS3-PS as set out in Table 6-1. Temporarily overloading the transformer above its nominal power rating during the ESCB (re-)charging phase may be considered under the condition that all relevant operating parameters (temperature, voltage drop, etc.) remain within their specified range and

that all relevant temperature hotspots are identified and considered in the overtemperature protection function (refer to section 6.4.3.9).

7.2.2.4 Enclosure

The transformer shall be enclosed in accordance with NF C 13-200.

7.2.2.5 Cooling

The transformer and/or the transformer enclosure shall be water-cooled to reduce heat rejection into the air.

7.2.2.6 Earthing

An IT earthing scheme shall be implemented downstream the secondary (LV) winding of the transformer. The implementation shall be in accordance with NF C 15-100 [CS25].

7.2.2.7 Protection

Each power transformer shall be protected by a dedicated protection relay.

7.2.3 AC/DC converter

In addition to the common requirements for power electronic switch modules specified in section 8.3.3, this section defines the specific requirements applicable to the AC/DC converter of the rectifier stage.

7.2.3.1 Input filter

The AC/DC converter shall incorporate an input filter to ensure compliance with PPEN requirements (see section 9.7, e.g. current harmonics) and all applicable standards, including those related to EMI.

7.2.3.2 Rectifier modules

If the rectifier consists of multiple rectifier modules connected in parallel, each module shall be equipped with a current sensor to monitor current-sharing performance during operation.

7.2.3.3 Pre-charge circuit

If a dedicated pre-charge circuit is implemented, it shall be designed to:
- limit the inrush current to values compatible with the ratings of the semiconductor devices, passive components, and protective devices;
- ensure a controlled transition from pre-charge mode to normal operation;
- prevent unintended bypass or short-circuiting of the pre-charge path.

If implemented, the current in the parallel pre-charge circuit shall be monitored by means of a dedicated current sensor.

7.2.3.4 Switching frequency

The switching frequency of the rectifier shall be defined by DA taking into account all performance requirements, efficiency and loss considerations, output filter constraints, harmonic and EMI considerations, and any other relevant design factors.

7.2.4 Output filter

The need for, and potential implementation of, a filter at the rectifier output shall be evaluated with respect to the output ripple requirements of the inverter, and the applicable EMI standards.

Sufficient capacitance shall be implemented locally at the output of the rectifier for the purpose of limiting transient voltage overshoot and reducing EMI, and a dedicated bleeder resistor shall be implemented to ensure the discharge of this capacitor within 5 hours.

A portion of the ESCB's required capacitance may be located at the rectifier output for aforementioned purpose, as per the provisions of section 7.3.1.2.

7.3 Energy Storage Capacitor Bank

This section defines the technical requirements applicable to the ESCB. Each of the two power converters incorporates a dedicated ESCB; therefore, all values specified herein (e.g., energy, capacitance) shall be understood to apply to a single ESCB.

7.3.1 Architecture

7.3.1.1 Hierarchical definitions

For the purposes of the following section, the hierarchical breakdown defined below and illustrated in Figure 7-3 shall apply.

Each Energy Storage Capacitor Bank is comprised of one or multiple ESCB modules connected in parallel. Each ESCB Module is subsequently composed of multiple ESCB cells. The ESCB cells are finally comprised of multiple physical capacitors.

Within this hierarchy, an 'ESCB cell' refers to the smallest unit of capacitance protected by a dedicated fuse for meeting the maximum energy requirements of section 7.3.3.3. An 'ESCB module' refers to an assembly of ESCB cells housed within a single, standalone enclosure.

Energy Storage Capacitor Bank
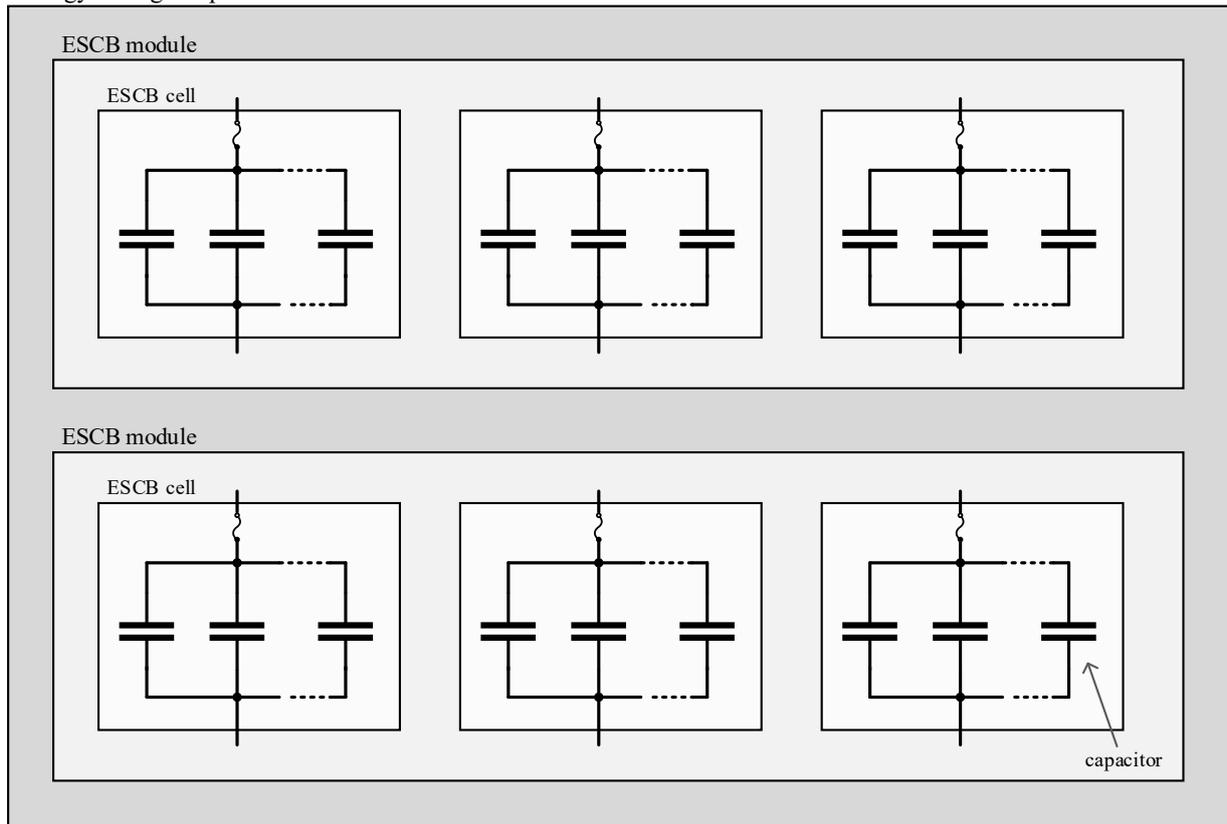
Figure 7-3: hierarchical definitions for the Energy Storage Capacitor Bank

7.3.1.2 *Transferring capacitance to the rectifier and inverter stages*

Part of the required ESCB capacitance may be physically located at the output of the rectifier and/or the input of the inverter, e.g. for local decoupling and limiting transient voltage overshoot and EMI.

In case the total energy of the outplaced capacitance exceeds the maximum energy of an ESCB cell as per the provisions of 7.3.3, the outplaced capacitors shall be considered as integral part of the ESCB including all electrical safety requirements thereof.

7.3.2 *Electrical requirements*

7.3.2.1 *Energy*

The net electrical energy storage capacity of the ESCB shall be the highest of:
- The energy required by the inverter stage to deliver the VDE pulse output waveform (as per 6.1.1.2) into the VS3-PS load (6-turn configuration), plus a margin of 10%
- 12 MJ [1]

Note 1: this minimum value shall not be interpreted as guaranteeing that the VDE-pulse current waveform can be achieved with (2x) 12 MJ.

The net energy capacity is defined as the electrostatic energy contained by the ESCB capacitance C between the nominal DC Link voltage $V_{dc(nom)}$ and the minimum DC Link voltage $V_{dc(min)}$ as follows:

$$E_{net} = \frac{1}{2} C\left(V_{dc(nom)}^2 - V_{dc(min)}^2\right) \# (1)$$

The minimum DC Link voltage depends on the design and operation of the rectifier stage design and should be considered in accordance with section 6.1.2.

Similarly, the gross energy is defined as:

$$E_{gross} = \frac{1}{2} C V_{dc(max)}^2 \# (2)$$

The maximum DC Link voltage should be considered in accordance with section 6.1.2.

All assessments related to the electrical safety of the ESCB shall be performed using the gross capacity of the ESCB.

7.3.2.2 Capacitance

The ESCB nominal capacitance shall be derived from the required net energy content and the DC Link operating levels as per equation (1) of section 7.3.2.1:

$$C_{nom} = \frac{2E_{net}}{\left(V_{dc(nom)}^2 - V_{dc(min)}^2\right)} \# (3)$$

The required nominal capacitance shall be defined based on:
- Actual ambient conditions (temperature, humidity)
- At the end of VS3-PS service life (considering negative capacitance drift)
- At DC$^+$ (1 mHz)

The variation of the ESCB capacitance with respect to the nominal capacitance shall not exceed ±5%, taking into account component tolerances, temperature and humidity, long-term drift, and non-replaceable component failures over the service life of VS3-PS.

The variation of the ESCB capacitance with frequency $\Delta C(f)/C_{nom}$ shall not exceed ±5% at 1 kHz.

7.3.2.3 Voltage

The ESCB shall be capable of operating at the maximum DC Link voltage $V_{dc(max)}$ for the specified operating and service life requirements (refer to section 6.2.2).
Each physical capacitor shall be capable of operating at the full ESCB voltage, i.e. no series connections.

7.3.2.4   Dielectric and technology

All capacitors incorporated into the ESCB shall be Metallized Polypropylene (MPP) dry-type capacitors.

The capacitors shall have self-healing capabilities. The expected loss of capacitance over the service life due to the resulting insulated regions shall be taken into account in the maximum capacitance variation of section 7.3.2.2.

7.3.2.5   Equivalent Series Resistance (ESR)

Given the specified capacitor technology, typically resulting in low ESR values, no specific requirements regarding the ESR apply. Nonetheless, the provisions on the internal impedance of section 8.4.1 are applicable.

7.3.2.6   Dielectric losses

Given the required capacitor technology, no specific requirements regarding the dielectric losses or loss tangent apply.

7.3.3   Electrical and occupational safety requirements

The ESCB contains a substantial amount of electrical energy once charged, and therefore the highest level of attention must be given in the design, control and operation to both electrical and occupational safety hazards.

This section contains requirements that aim at reducing the electrical and occupational hazards, nevertheless the full compliance with all applicable norms and the final safety demonstration remain the full and sole responsibility of the DA.

7.3.3.1   Segmentation

The ESCB shall be segmented into modules and cells as per Figure 7-3.

7.3.3.2   Passive overcurrent protections (fuses)

Fuses shall be implemented for overcurrent protection such that no hazards and permanent damage result from capacitor failures, power converter component failures and control malfunctions.

7.3.3.2.1   Cell fuses

Each cell shall be equipped with a fuse for overcurrent protection.

7.3.3.2.2   Global fuse

In addition to fuses at cell-level, global fuses shall be implemented at the ESCB-level, in accordance with the SLD [RD50].

7.3.3.2.3 Selectivity

The overcurrent protection through fuses shall be selective. In the event of a capacitor failure, only the fuse associated with the affected cell shall operate. In the event of a failure or control error on the power converter side, only the ESCB-level fuse shall operate.

7.3.3.2.4 ESCB module protections

The need for overcurrent protections at the ESCB module-level shall be assessed by DA in accordance with risk and electrical safety assessments.

7.3.3.3 Maximum energy

7.3.3.3.1 Maximum energy per cell

The maximum energy contained by any ESCB cell shall be limited by design to 100 kJ.

7.3.3.4 Bleeder resistance

Each cell shall be equipped with a bleeder resistor that discharges the entire cell from $V_{dc(max)}$ to <50V within 5 hours, even when isolated from the ESCB by e.g. a tripped fuse.

The bleeder resistance shall be sufficiently low to minimize any recovery voltages that may appear due to dielectric polarization processes.

7.3.3.5 Design implications on other VS3-PS components

The design of all cables and enclosures part of the VS3-PS power circuit, and in particular those directly connected to the DC Link, shall explicitly account for the risks associated with arc-flash and arc-blast resulting from electrical faults, taking into consideration the substantial energy stored in the ESCB.

7.3.3.6 Voltage Absence Test

All necessary design provisions, accessibility features, and safety interfaces shall be incorporated to enable the performance of Verification of Absence of Voltage (VAT) tests in full compliance with NF C 18-510 [CS26]. This includes, among others, ensuring adequate accessibility to test points, sufficient clearance to apply a VAT device without risk of inadvertent contact with live parts, incorporating isolators with visible break, etc.

This requirement applies to every subsystem of VS3-PS; the DA shall, however, give particular attention to the design of the ESCB, its modules and its cells to ensure full conformity with these obligations and with NF C 18-510 [CS26] in general. Any rectification measure to address the VAT issue identified during the Regulatory Inspection can be costly and time consuming.

7.3.4 Enclosures

The enclosures of the ESCB shall comply with all system-level requirements of section 8.5. This section contains specific supplementary requirements for the ESCB.

7.3.4.1 Material

The outermost ESCB enclosures shall be constructed from steel.

7.3.4.2 *Arc-blast withstand capability*

The outermost ESCB enclosures shall be designed and constructed to fully contain any arc-flash resulting from a fault or malfunction and to withstand the associated arc-blast without incurring structural plastic deformation.

7.3.4.3 *Capacitor casing*

Capacitors with steel cases shall be used for the ESCB.

The tightness and integrity of the capacitor casing shall remain fully preserved under all fault conditions, including any electrical arc-flash event. No degradation, loss of sealing performance or compromise of enclosure integrity shall be permitted.

7.3.5 *Safety Design Verifications*

The DA shall demonstrate, through comprehensive and duly documented verification activities, the safety of the Energy Storage Capacitor Bank and of the VS3 Power Supply into which it is integrated. The DA shall in particular address the hazards associated with explosive arc-blast phenomena arising from electrical arc energy.

At a minimum, the following activities shall be performed and documented.

7.3.5.1 *Identification of fault scenarios*

Comprehensive short-circuit analyses shall be conducted at both the system level and within the Energy Storage Capacitor Bank. These analyses shall evaluate all credible fault conditions in order to identify the resulting arc-energy scenarios to be used as input for subsequent explosion modelling, including CFD-based or equivalent analytical methods.

7.3.5.2 *Arc flash scenario analyses*

The DA shall perform CFD-based or equivalent analytical evaluations to assess the effects of arc-energy release under the identified short-circuit scenarios. These evaluations shall address, at a minimum, enclosure structural integrity, internal pressure rise, and arc-propagation behaviour, and shall demonstrate the ESCB design is safe and passes clearly defined and justified acceptance criteria.

7.3.5.3 *Short-circuit tests on ESCB cells*

Short-circuit tests shall be conducted on the elementary ESCB cell to verify its fault-current interruption capability, to quantify the electrical energy released during the fault, and to demonstrate both the structural integrity of the capacitor enclosures and the absence of damage to the capacitors.

The test conditions and the associated pass/fail acceptance criteria shall be explicitly defined and agreed with IO prior to the execution of any tests.

7.3.6 Monitoring

The VS3-PS shall monitor all essential ESCB performance and state parameters in accordance with the requirements of section 7.9.1. Given that the pulsed operation requires a defined minimum amount of energy, the primary purpose of this monitoring is to ensure sufficient energy is available for plasma control actions.

As a minimum, the following monitoring features shall be implemented.

7.3.6.1 State-of-health

The VS3-PS shall implement State-of-Health (SoH) monitoring of the ESCB to quantify any degradation in capacitance with a precision and accuracy of 1% of the nominal capacitance. As a minimum, the operational status of each ESCB cell shall be monitored, either via fuse-trip indication (e.g., microswitch or voltage-based detection) or through direct cell-level measurements (e.g., cell-voltage or cell-current monitoring).

7.3.6.2 State-of-charge

The VS3-PS shall implement State-of-Charge (SoC) monitoring of the ESCB to quantify, in real time, the energy available for any upcoming operating pulse, with a precision and accuracy of 2% of the nominal net energy.

7.4 DC Link

The DC Link interconnects the rectifier, inverter and ESCB modules. This section specifies the requirements for equipment operating at the DC Link level.

7.4.1 Overvoltage Protection

An overvoltage protection mechanism (e.g. crowbar) shall be implemented at the DC Link level to safeguard the connected VS3-PS components, as well as the load circuit, against overvoltage conditions. The mechanism shall, in particular, prevent DC-Link overvoltage resulting from power converter control failures, from inductive energy in the load circuit being returned to the DC Link, and from voltages induced via the coil circuit.

The DA shall define the ratings and dynamic performance of the overvoltage protection mechanism to ensure adequate protection against all identified scenarios.

The overvoltage protection mechanism shall allow external triggering via a command issued by the PIS, in addition to a self-triggering mode activated at a predefined voltage threshold.

The overvoltage protection mechanism shall be capable of operating in the absence of SSEN Class IV supply.

The operation of the overvoltage protection mechanism, including self-triggering, shall be interlocked with the global emergency stop function of the power supply.

7.4.2 Discharge systems

7.4.2.1 Regular discharge

The DC Link shall be equipped with a mechanism capable of discharging all its capacitive energy and all excess energy originating from the VS3 load circuit and from induced current events. The discharge time shall be compatible with the operation schedule as per section 6.2.2.

The option of reverse power flow through the rectifier stage (i.e. regenerative discharge) may be considered; however, the need for a backup discharge mechanism – such as in the event of loss of AC power – shall be evaluated in accordance with the FMECA.

7.4.2.2 Fast discharge

The DC Link shall be equipped with a fast discharge system capable of discharging the DC Link, including all capacitive energy of the rectifier output stage, the ESCB and inverter input stage, in accordance with the performance requirements specified in Table 6-3.

The fast discharge system shall incorporate a normally-on switching element such that the discharge is automatically initiated upon loss of power.

The fast discharge switch shall be supplied from SSEN Class II-IP or Class IV, as determined by the outcomes of the FMECA.

The operation of the fast discharge mechanism, either actively or passively due to loss of supply voltage, shall be interlocked with the global emergency stop function of the power supply.

The recovery time following a fast discharge event shall not exceed 30 minutes.

The required number of operating cycles shall be determined in accordance with the FMECA and shall be no fewer than 1000 cycles.

7.4.2.3 Bleeder resistors

All energy storing components connecting to the DC Link shall be equipped with their own bleeder resistors; consequently, no dedicated bleeder resistors are required at the DC Link itself. However, if additional components are incorporated into the DC Link, or if substantial cable lengths are present, then supplementary bleeder resistors shall be included at the DC Link to ensure proper discharge of such components and cables.

7.5   Inverter Stage

7.5.1   Input circuit

7.5.1.1   Overcurrent protection

Each inverter module shall be equipped on the input-side with an overcurrent protection device or mechanism (e.g. fuse) capable of protecting the module from overcurrent conditions and from short-circuit currents in case of faults and erroneous control signals.

The status of the overcurrent protection mechanism or device (e.g. fuse) shall be continuously monitored and reported to the VS3-PS PIS, which shall execute the corresponding protective or operational actions.

The need for overcurrent protection for switch modules and individual switch devices shall be assessed by the DA and implemented as required.

7.5.1.2   Input filter and capacitance

The need for, and potential implementation of, a filter at the inverter input side shall be evaluated.

Sufficient capacitance shall be implemented locally at the input of each inverter module to limit transient voltage overshoot such that the lowest voltage class can be selected, to reduce the current ripple conducted over the DC link cables and to reduce EMI. A dedicated bleeder resistor shall be implemented to ensure the discharge of this capacitor within 5 hours.

A portion of the ESCB's required capacitance may be located at the input of the inverter modules for aforementioned purpose, as per the provisions of section 7.3.1.2.

7.5.2   DC/AC converter

In addition to the common requirements for power electronic switch modules specified in section 8.3.3, this section defines the specific requirements applicable to the DC/AC converter of the inverter stage.

7.5.2.1   Switching frequency and modulation

The switching frequency of the inverter shall be defined by DA taking into account all performance requirements, efficiency and loss considerations, output filter constraints and EMI considerations, and any other relevant design factors.

Interleaved operation between the two power converters and/or the parallel inverter modules comprising them shall be evaluated and applied as appropriate to reduce voltage and current ripple, minimise EMI, and potentially enhance transient-response performance.

7.5.2.2   Inverter modules

The number of inverter modules shall be defined by the DA taking into account all performance requirements, the optimization of effective switching frequency, and any modular design constraints, including those related to enclosures (refer to section 8.5).

Each inverter module shall be equipped with a current sensor to continuously monitor current-sharing performance during operation.

7.5.2.3 Switch modules

The required number of parallel switch modules shall be determined by the DA taking into account, among other factors, the maximum virtual junction temperature (section 8.3.3.3) and, in particular, the junction temperature variation (ΔT_j) resulting from the pulsed operating modes. The design shall ensure that the resulting thermal cycling profile is compatible with the required service life.

7.5.2.4 Gate control signals and gate drives

All switching signals that directly control the gate(s) of the switching modules shall be routed through dedicated gate-enable logic.

The associated enable signal (active-high) shall be hardwired and interfaced with the PIS to support interlock functions requiring immediate and high-reliability shutdown of the power converters, including, for example, overcurrent protection with activation of the crowbar system.

The gate-enable logic may be implemented in hardware by an enable circuit or through FPGA- or software-based solutions. Regardless of the implementation, it shall achieve the integrity level required by the classification of the interlock function it serves.

Hardware-based solutions may include dedicated enable circuits such as latches, the integrated enable feature in the fibre-optic transceivers transmitting the gate signals (if any), or the use of gate drivers that incorporate an integrated enable feature.

Software-based solutions may include the programming of such enable logic or enable circuit directly in the microcontroller or FPGA generating the gate signals, respectively.

7.5.3 Output filter

An output filter shall be implemented at the output of the inverter stage to reduce the voltage slew-rate (dv/dt), for reducing the currents in the busbar/coil circuit's stray capacitance, and for minimizing the current ripple and EMI in general.

The output filter shall filter both differential and common-mode disturbances, in accordance with applicable EMI standards.

7.5.3.1 Attenuation of switching harmonics

The attenuation of the voltage component of the first switching harmonic shall be at least 30dB in differential mode.

The filter shall contribute to limiting the output current ripple in accordance with the value stated in Table 6-1.

7.5.3.2 Maximum slew-rate

The differential-mode voltage slew-rate (dv/dt) at the output of the power supply shall be limited to 50 V/us. This value envelopes the slew-rate limitation of the VS-coils (refer to section 9.2.2.3).

Common-mode voltage transients shall be limited in accordance with applicable EMI standards.

7.5.3.3 Performance constraints

The insertion of the output filter shall not degrade the dynamic performance or introduce excessive impedance at the relevant operating frequencies.

The output filter shall not compromise the required transient voltage response time of 1 ms stated in Table 6-1.

In accordance with section 8.4.1, the additional (series) impedance introduced by the filter shall not significantly affect the power supply performance, in particular in relation to the generation of the VDE pulse waveform.

7.5.4 Resistive earthing system

A resistive earthing system shall be installed at the output of each power converter, for the purposes of:

- Establishing a symmetrical potential of the output terminals with respect to earth
- Enabling the detection of earth-fault conditions within the power supply and its associated load circuit

7.5.4.1 Monitoring and detection of earth faults

An earth-fault monitoring and detection system shall be implemented to ensure continuous supervision of insulation integrity across the entire power supply circuit.

The system shall detect both high-impedance and low-impedance earth-fault conditions, provide clear indication of fault presence to the Plant Interlock System, such that the latter can initiate protective actions in accordance with the defined safety logic of the interlock function (refer to section 6.4.3.8).

The detection thresholds, response times, and coordination with other protection functions shall be defined to ensure reliable operation under all normal and transient conditions, including energization, discharge events, and load circuit dynamics.

The earth-fault monitoring system shall remain fully operational during all modes of operation.

7.5.4.2 Implementation

The implementation of the earth-fault protection shall be compliant with NF C 13-200 [CS24] and/or NF C 15-100 [CS25] and preferably make use of COTS devices. The integrity level of the protection devices shall correspond to the integrity classification of the interlock function(s) they support.

7.6 Crowbar Requirements

A current bypass device, hereinafter referred to as crowbar, shall be implemented at the output of each power converter to:

- divert fault currents originating from the power supply for protection of the coil circuit, and to
- divert induced overcurrent in the coil circuit arising from transient plasma events for the protection of the power supply.

7.6.1 Control

The crowbar functions as an actuator within the Plant Interlock System, including for overcurrent protection (section 6.4.3.4), where it typically serves as the final layer of protection.

7.6.1.1 Integrity level

The integrity level of the crowbar system shall correspond to the integrity classification of the interlock function(s) it supports.

Where parallel switching devices are employed, they should preferably be implemented as fully independent parallel branches with respect to both control and thermal management. The number of branches shall provide sufficient margin to accommodate current imbalance and potential branch unavailability.

7.6.1.2 Crowbar operation

The crowbars of the two power converters shall be operated in unison, with the sole exception of their passive overvoltage protection function.

7.6.2 Functional requirements

The crowbar system shall implement two concurrent operating modes, namely externally triggered operation under control of PIS, and self-triggered overvoltage protection.

7.6.2.1 Operation under command of PIS

The crowbar system shall become fully conductive within no more than 1 ms following a trigger command from the PIS. Once triggered, the crowbar system shall remain in a conductive state until the current has fully decayed.

7.6.2.2 Self-triggered overvoltage protection

The crowbar system shall incorporate a self-triggered overvoltage protection function that triggers autonomously when the power convert output reaches a predefined threshold. This threshold shall be defined by the DA so as to provide maximum protection against overvoltage while preventing spurious activation under elevated but nominal output voltage conditions, and shall in all cases be consistent with the outcomes of the FMECA.

The self-triggered overvoltage protection shall remain fully operational in the event of a loss of Class IV supply.

The crowbar system shall include a means of reading back the instantaneous conduction state of the switching device through a dedicated transducer (e.g. a Rogowski coil) for detection of the activation state.

In accordance with the provisions of sections 6.4.1.1 and 6.4.3.5, the status of this self-triggered protection shall be reported to PIS/CIS.

7.6.2.3 Interlocking with converter operation

Triggering of the crowbar system, whether through passive or active means, shall be interlocked with the inhibition of the switching signals by means of the provisions of sections 7.5.2.4 and 6.4.3.12.

Upon activation of the crowbar – passively or actively – all controllable switches of the H-bridges in the inverter stage shall be placed in a non-conductive state.

7.6.3 Performance requirements

The crowbar system shall be capable of conducting current in both directions and shall withstand blocking voltages of either polarity.

7.6.3.1 Current rating

The crowbar system shall be capable of withstanding the maximum of:

a) The highest induced current in the coil circuit plus a margin of 25%

b) The maximum fault current of the VS3 Power Supply plus a margin of 20%

The maximum induced current in the coil circuit is estimated at 95.4 kA for 6-turn operation (see section 6.6.3), hence the minimum operational current withstanding level shall be 120 kA.

The duration and relevant waveforms shall be derived from the power supply fault scenarios and from the induced current waveforms, both with sufficient margin to satisfy the required integrity levels.

7.6.3.2 Thermal requirements

The crowbar system shall be capable of operating in the absence of cooling water for a single actuation event.

The recovery time after an actuation event shall be less than 30 minutes, under nominal cooling conditions.

7.6.4 Service life

The number of actuation events that the crowbar system must be capable of performing shall be defined in accordance with the FMECA. As a minimum requirement, the crowbar system shall be capable of performing 3,000 actuation events, comprising both interlock-initiated actuations and self-triggered overvoltage protection actuations.

7.7 Mechanical Switching Elements

Sufficient earthing and disconnect switches shall be implemented to ensure compliance with applicable regulations and to support commissioning, troubleshooting and maintenance activities. As a minimum requirement, the earthing and disconnector switches identified in the SLD shall be implemented.

7.7.1   General requirements

7.7.1.1   Voltage rating

The mechanical switches shall be rated for the full system voltage in accordance with insulation coordination requirements (section 8.1). Their nominal operating voltage rating shall be no less than the highest of the following:

- maximum AC input voltage,
- maximum DC link voltage,
- maximum load voltage,
- maximum induced voltage in the load circuit, and
- maximum test voltages (including those specified in section 8.1)

Both normal and faulty operating conditions shall be considered.

Adequate margin shall be provided, in accordance with applicable standards.

7.7.1.2   Configuration

The disconnect switches shall open all three poles for AC power connections and both poles for DC connections. The earthing switches shall connect all relevant poles to ground.

7.7.1.3   Switch operation

7.7.1.3.1   Remote control

All disconnect switches shall be motor-operated and capable of remote control. Reconfiguration of the circuit (off-load) through remote operation of the disconnector(s) shall be achievable without the need for physical access.

7.7.1.3.2   Manual operation

The disconnectors shall provide the capability for manual operation, thereby allowing local override of remote control.

The disconnectors shall be equipped with a physical mechanism that secures them in a defined position (e.g., trapped-key system or an equivalent solution).

7.7.1.3.3   Occupational safety considerations

The remote control of the mechanical switches does not contribute to occupational safety. Therefore, the control from conventional control systems is permitted. This is in agreement with the strategy disclosed in [RD58].

7.7.1.4   Switch state monitoring and avoidance of hazardous configurations

The physical switch position of each mechanical switch shall be monitored (e.g., through limit switches) and shall be integrated into the relevant interlock functions (e.g., the system integrity interlock in 6.4.3.12).

Hazardous configurations shall be actively prevented, including but not limited to:

- Opening disconnectors while system is energized (on-load switching)
- Closing earth switches while system is energized

7.7.1.5 *Interlocking disconnectors and earthing switches*

Operation of the earthing switches in the output circuit shall not necessarily be interlocked with the operation of the associated disconnector switch.

The configuration of the output disconnector switch and the output earthing switch during shutdown and maintenance states shall be assessed as part of the FMECA, taking into account the possibility of the TF-coil circuit remaining energized and the risk of induced currents arising from transient events such as fast discharges.

7.7.2 *Disconnect Switches*

Sufficient disconnect switches shall be implemented to ensure compliance with applicable regulations and to support commissioning, troubleshooting and maintenance activities.

7.7.2.1 *Minimum set of disconnect switches*

As a minimum, the following disconnector switches shall be implemented, as identified in the SLD [RD50].

7.7.2.1.1 AC disconnector

A disconnector shall be implemented directly downstream the secondary winding of each power transformer.

7.7.2.1.2 Load circuit disconnector

A disconnector shall be implemented directly downstream the dummy load branch and upstream the load circuit voltage measurement of each power converter (refer to [RD50]).

7.7.2.1.3 Dummy load disconnector

Disconnect switches shall be implemented in the dummy load branch at each power converter side, directly downstream the main power converter poles (refer to [RD50]).

7.7.3 *Earthing Switches*

Sufficient earthing switches shall be implemented to ensure compliance with applicable regulations and to support commissioning, troubleshooting and maintenance activities.

7.7.3.1 *Minimum set of earthing switches*

As a minimum, the following earthing switches shall be implemented, as identified in the SLD [RD50].

7.7.3.1.1 AC earthing switch

An earthing switch shall be implemented directly upstream the AC/DC converter of the rectifier stage.

7.7.3.1.2 DC Link earthing switch

An earthing switch shall be implemented directly upstream the DC/AC converter of the inverter stage.

7.7.3.1.3 Output earthing switch

An earthing switch shall be implemented downstream the DC/AC converter of the inverter in accordance with the SLD [RD50].

7.7.3.1.4 Load circuit earthing switch

An earthing switch shall be implemented directly downstream the current measurement that is closest to the VS3 extension busbar interface point, as per the SLD [RD50].

7.7.3.1.5 Dummy load earthing switch

An earthing switch shall be implemented in the dummy load branch to provide earthing of the dummy load when it is not in service.

7.8 Dummy Load Requirements

The VS3 Power Supply system shall comprise a permanently installed dummy load for test and commissioning activities.

7.8.1 Configuration and connections

The dummy load shall comprise two branches, each containing a series RL-circuit with half the required dummy load resistance and half the inductance. The two branches shall be inserted in the power supply output circuit through mechanically operated switches as shown in the SLD [RD50].

The DA shall design and supply all necessary cables and/or busbars, as well as the connection systems.

7.8.2 Operation and protection

Operation on dummy load is a specific configuration used for commissioning and maintenance activities, which permits to operate the power supply out-of-pulse. The position of the mechanical switches for the dummy load and those for the regular load circuit shall be monitored and reported. In particular, the on-dummy load position switch is a protection signal to be reported to CIS.

7.8.3 Impedance magnitude and phase

The dummy load impedance shall reasonably approximate the VS3-PS electrical load with the VS-coil in 6-turn configuration.

The impedance magnitude at 0.1 Hz shall be approximately (±10%) equal to that of the 6-turn load circuit at the same frequency.

Should specific interface or integration aspects require so, the impedance phase may be adapted to relieve the design and integration of the dummy load. This may involve reducing the inductive component, while increasing the resistive impedance component. As a minimum, at least 15% of the equivalent load inductance shall be retained. The final adaptation is to be agreed with IO.

In all cases, the impedance magnitude and phase of the dummy load shall be selected such that the voltage and current waveforms of the dummy load resemble those of the real VS3 load circuit for in particular the 80 kA VDE pulse.

7.8.4 Electrical ratings

The voltage and current ratings of the dummy load shall take into account FAT, SAT and troubleshooting needs. The rated operating voltage shall not be less than 2400V, the current rating shall allow for both noise operation and pulsed operation up to 80 kA in accordance with the performance specifications in Table 6-1.

7.8.5 Operating duty cycle and service life

The dummy load shall be designed for an operating duty similar to VS3-PS.

The design life of the dummy load shall not be less than the design life of VS3-PS. The required number of operating hours shall be determined on the basis of the commissioning and maintenance plans, with appropriate margin.

7.8.6 Electromagnetic and environmental requirements

7.8.6.1 Core saturation

In case magnetic cores are used

The saturation current of the inductor magnetic core, if any, shall be equal or greater than 5 times the maximum output current of the power supply. At this level of current, the inductance of the inductor may be reduced by 80%.

7.8.6.2 Stray fields

The stray (electro)magnetic field emitted by the inductor of the dummy load shall be taken into account into the analysis of EMI and electromagnetic loads.

7.8.6.3 Power dissipation and cooling

The power dissipated in the dummy load, in particular in case of an increased resistive component under the provisions of section 7.8.3, shall be carefully assessed and considered in the heat loads to the building and heat released into the cooling water circuit.

At least 80% of the instantaneous heat generated by the dummy load shall be rejected to the cooling water system.

Given the significant cooling water flow required, an isolation valve shall be implemented for isolation during normal (non-dummy load) operation.

7.9 Instrumentation & Control Requirements

The design, implementation of the VS3-PS I&C system shall be compliant with the Plant Control Design Handbook [AD46] and its applicable documents. Deviations shall be recorded as Deviation Requests.

This section emphasizes on the most important and most impacting requirements as well as specific requirements.

7.9.1 Instrumentation

Sufficient instrumentation shall be included in the VS3-PS plant system, to monitor component performance, system state, integrity and interlock within the design envelope, in order to ensure human safety/security, to record all system control actions, and to warn plant operators of the onset of operation outside the design margins, or of any off normal event.

7.9.1.1 Instrumentation for plasma control and ITER as integrated system

7.9.1.1.1 Measurements

In addition to all instrumentation required for internal control, the VS3 Power Supply shall provide all voltage and current signals that are essential to plasma control and the operation of ITER as an integrated system, including but not necessarily limited to:

- Current measurements for each power converter
  - o Coil circuit current - one current sensor downstream the crowbar
  - o Inverter output current – one current sensor directly upstream the crowbar
- Voltage measurements for each power converter
  - o Inverter output voltage – one voltage sensor immediately downstream the inverter
  - o ESCB voltage – one voltage sensor immediately downstream the capacitor bank
- Voltage measurements for VS3 Power Supply
  - o Coil circuit voltage – as combination of the inverter output voltages, or, VS3U/VS3L voltages

These measurements are listed for functional purposes and do not necessarily reflect the required provisions for reliability, availability and fault tolerance of the sensors involved in investment protection functions. In particular, the integration of three interlock-grade sensors measuring the coil-circuit current should be considered.

Measurements for plasma control downstream the power supply – extension busbar interface point are not required, nor foreseen.

Without prejudice to the completeness of the list for the purposes of this requirement, Figure 7-4 shows the aforementioned measurements for plasma control and operation of ITER as integrated system.
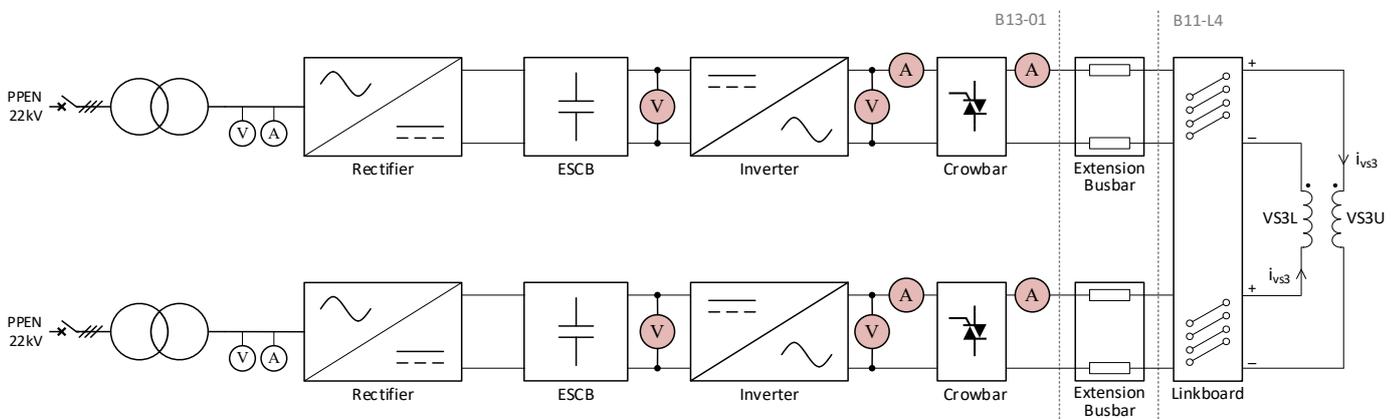
Figure 7-4: high-level diagram with measurements included for plasma control / ITER operation

Additional instrumentation shall be provided as required, for the operators to measure, monitor and troubleshoot the performance of the VS3 Power Supply.

The segregation of signals for plasma control and operation shall be provided.

7.9.1.1.2   Performance requirements

The VS3 Power Supply shall provide the voltage and current signals under the provisions of 7.9.1.1.1 with the performance characteristics specified in Table 7-1.

Table 7-1: Performance and technical requirements for plasma control related measurements

	Plasma control measurements [1]	Monitoring measurements [1]
Signals	- *VS-coil current* - *PS output voltage*	- *PS output current* - *PS DC link voltage*
Range	VS coil current: 0…±120 kA PS output voltage: 0…±3 kV	As per VS3-PS needs
Accuracy [2]	≤ 0.5% of FSR (current) < 1% of FSR (voltage)	≤ 5% of FSR
Precision	DR ≥ 80 dB SNR ≥ 60 dBFS	DR ≥ 50 dB SNR ≥ 50 dBFS
Bandwidth (-3dB)	Current: DC … ≥ 0.5 kHz [1] Voltage: DC … ≥ 1 kHz	DC … ≥ 100 Hz
Data rate [3]	Current: ≥ 4 kHz Voltage: 10 kHz	≥ 1 kHz
Delay	≤ 1 ms	≤ 10 ms

Note 1: Control measurements are those considered relevant for the real-time control of the vertical stabilization of the plasma, including closed-loop control at PCS. Monitoring measurements are those related to the operation of the power supply system and are provided to PCS for allowing estimation of the power supply status. The performance requirements on Monitoring measurements are considered as minimum; the actual performance may be better depending on the detailed design of the power supply.

Note 2: the accuracy specification considers all mechanisms contributing to measurement uncertainty that cannot be compensated or calibrated for, including but not limited to: nonlinearity error, gain error drift and offset error drift. Static gain and offset errors are assumed to be compensated/calibrated for and are not included in the stated accuracy.

Note 3: the data rate specifies how frequently data is to be provided, it does not necessarily correspond to the sampling rate, which may be considerably higher.

7.9.1.2   *Instrumentation for internal control and monitoring purposes*

Sufficient instrumentation shall be included in the VS3-PS plant system, to monitor component performance, system state, integrity and interlock within the design envelope, in order to ensure human safety/security, to record all system control actions, and to warn plant operators of the onset of operation outside the design margins, or of any off normal event.

The measurements shall provide the information necessary for troubleshooting purposes, with an adequate level of detail and update interval.

7.9.2   I&C Architecture

The conceptual control architecture for the VS3-PS System is given in [RD21] and depicted in Figure 7-5. This architecture is consistent with the Interface Sheet between the VS3-PS System and CODAC [AD84].

This control architecture shall be considered as a proposal from IO, the DA may deviate and define alternative architectures as long as all technical and interface requirements are met.
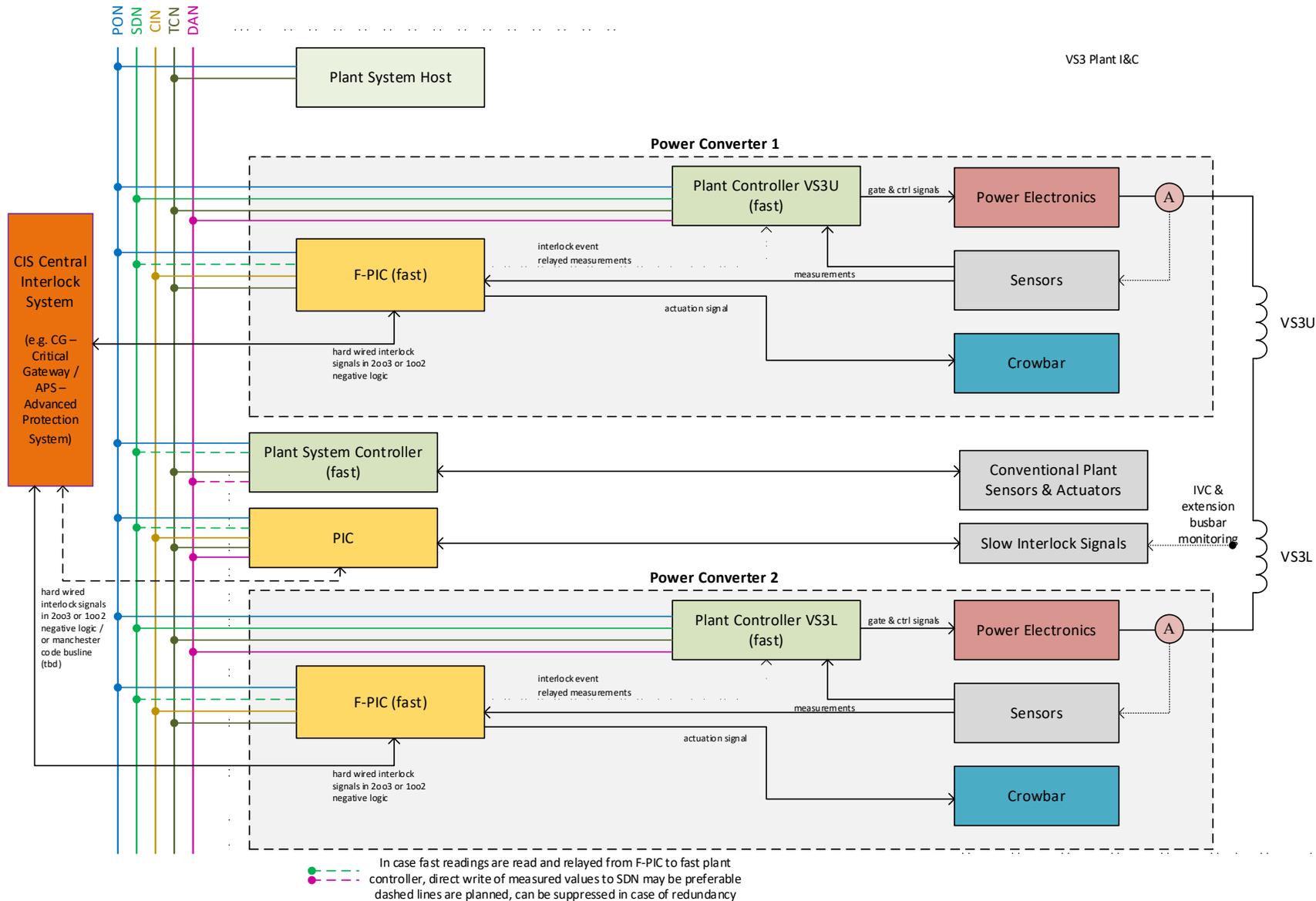
Figure 7-5. conceptual architecture of the VS3-PS converter I&C system [RD21]

7.9.3 General

The VS3-PS I&C systems shall be designed and implemented so that the functional requirements and interface requirements are met.

The following two types of control systems shall be implemented:

1. VS3-PS Interlock control systems.
2. VS3-PS Conventional control systems.

7.9.3.1 Separation of control

The clear separation of control, interlock and safety into three tiers shall follow the recommendation in the Plant Control Design Handbook [AD46].

7.9.3.2 Monitoring and control

The VS3-PS I&C systems shall perform real-time monitoring and control of each power converter and other subsystem of VS3-PS.

All control measurements, variables and states shall be communicated in real-time at their original sample time to the ITER Central Control System:

1. Control measurements refer mainly to the measurements of physical values like voltage, current and temperature and do typically not include control signals of power semiconductors (and the like)
2. If the real-time transmission is not possible, the data shall be recorded and timestamped by an autonomous and local transient recorder using the TCN time. This does not apply for signals required for the closed loop control with PCS.
3. The DA shall determine the variables required for the VS3-PS power converter troubleshooting and include them as part of the local timestamped records.
4. The transient recorder shall transfer transient record data automatically to the ITER Central Control System (not necessarily in real time).
5. The list of signals shall be provided by the Contractor and agreed by the IO in the design stage.

7.9.3.3 Interface with Protective relaying systems

Protective relaying systems shall be independent from the Local Control System (LCS) and Local Control Cubicles, but shall have an interface with them, for the purpose of status indication and interlocking.

7.9.3.4 Local control

Local control shall be instigated only on hand-shake permission, and key interlock administered from ITER's main control room.

Local control shall only be permitted in exceptional circumstances (such as local commissioning), but all signals and alarms shall always be visible from the ITER main control room. In local control mode, the VS3-PS control system shall maintain all monitoring and interlock functions.

The VS3-PS shall be capable of autonomous "local" control, as well as operation under supervisory control by PBS 45 CODAC. Local control shall include any, and all, features necessary for dummy load testing, without reliance on CODAC.

7.9.3.4.1 Local Human Machine Interface

The VS3-PS I&C systems shall include local control Human Machine Interface(s) (HMI), including measurements, variables and states normally communicated in real-time to the Central Control System.

The HMI shall report and display the global status and configuration of the main VS3-PS system, as well as the status of its power converters and other subsystems (state machine, measurements, control variables, etc.).

7.9.3.5 Human Machine Interface

The DA shall develop and provide the Human Machine Interface (HMI) based on Control System Studio (CSS) to the ITER Central Control System.

7.9.3.6 Time synchronization

All local clocks of controllers, especially the ones used to determine the timestamps of measurements, shall be synchronized with the ITER Central I&C System, or CODAC as described in PCDH [AD46], based on a central ITER clock distributed via TCN.

The time synchronization details are to be defined and agreed during the design phase and described in the design report.

7.9.4 Conventional control

7.9.4.1 Conventional control functions

The VS3-PS conventional control system(s) shall be implemented to provide the following functions, but not limited to:

1. Receive and process the voltage/current setpoints sent from the PCS via SDN.
2. Distribute the voltage/current setpoints from the SDN interface point to the controllers to the concerned VS3-PS actuators.
3. Control the VS3-PS system to generate the requested voltage and/or current.
4. Send high precision timestamped measurements of current and voltage with the defined real time sampling to the PCS via SDN.

7.9.4.2 State machines

The conventional control system shall implement a state machine for the subsystems of the VS3-PS System:

1. The state machines shall be independent for each of the two VS3-PS power converters
2. These state machines should have a similar level of detail as, and be linked with, the main state machine
3. The main state machine and subsystems' state machines shall be defined during the design activities and agreed before the Final Design Review.

7.9.4.3 Interface with CODAC

The conventional control system(s) of the VS3-PS System and Subsystems shall be interfaced with the ITER Central Control System, in accordance with the requirements defined in section 9.10.1.

As defined in the interface sheet with CODAC [AD84], IO will provide a development kit and a mini-CODAC system, to facilitate the tests (during FAT, can be used during SAT and commissioning according to project convenience agreed upon by the parties) and the integration of the VS3-PS system in the ITER Central Control system.

7.9.4.4 Fast Conventional Control

The following control functions shall be implemented on fast conventional controller(s) with the required sampling time:

1. Function(s) that receive or process the voltage and currents setpoints provided by the Plasma Control System (PCS) via SDN,
2. Function(s) that control the VS3-PS actuators based on the setpoints received by the PCS,
3. Function(s) that process and send the voltage and current measurements to the PCS via SDN.

Fast conventional controller(s) are interfaced with the Synchronous Databus Network (SDN), TCN (for time reference) and PON (for control).

7.9.4.5 Slow Conventional Control

Slow Conventional controllers can be implemented for slow tasks, e.g. configuration and supervision of the VS3-PS power converters. In that case, the slow conventional controllers are interfaced with the Plant Operation Network (PON).

7.9.4.6 Implementation – hardware selection

The DA shall implement the conventional controller(s) defined in the following documents and using the hardware as suggested in the ITER catalogues. Deviations shall be described and recorded:

- Plant Control Design Handbook [AD46],
- ITER catalogue for I&C products - Slow controllers PLC [RD23],
- Catalogue for I&C products – Fast controllers [RD24]

The products mentioned in these documents are compatible with the ITER Central Control System, certified, tested and used in existing plant systems.

The systems mentioned in the catalogues are already qualified for the ITER environment (Static Magnetic Field…) and do not require further qualifications.

If the DA selects and integrates products from the aforementioned catalogues, they will not be required to manage spare parts and obsolescence associated to those products.

If the DA selects other products, then they shall demonstrate that the proposed products are compatible with the ITER Central Control System and have equivalent performance. The required certifications or tests shall be provided.

The ITER catalogue could be updated in mutual agreement with the DA.

7.9.5   Interlock control

This section specifies the technical requirements applicable to the design and implementation of the control system supporting the Investment Protection (interlock) functions of the VS3 Power Supply. It complements the operational requirements defined in Section 6.4 and establishes the constraints under which the interlock control shall be realised from an architectural, functional and integration perspective.

Interlock control is distinct from conventional control in purpose and constraints. While conventional control regulates the performance of the power supply, interlock control is dedicated to the deterministic enforcement of protective actions in response to hazardous conditions, in accordance with ITER Investment Protection rules and architecture.

The design and implementation of the Plant Interlock System and associated functions shall comply with:

1. ITER Investment Protection Handbook [AD48]
2. Guidelines for the Design of the Plant Interlock System (PIS) [RD11]
3. Guidelines for PIS configuration and integration [RD12]

These documents constitute the normative technical references for the design, configuration and integration of the VS3-PS Plant Interlock System within the ITER interlock architecture.

Where applicable, the Standard PLC Template for Interlock Applications [RD9] should be considered for the development of the interlock control program(s).

7.9.5.1   Design and Integration

7.9.5.1.1   Architecture

The interlock control architecture for VS3-PS shall be implemented as a Plant Interlock System integrated into the ITER interlock hierarchy and interfaced with the Central Interlock System (CIS). It shall support the execution of local interlock functions protecting VS3-PS equipment, the coordination of protection actions involving common equipment and interfaces, and the exchange of interlock states, events and commands with CIS in accordance with the applicable Interface Control Documents.

The design and partitioning of the interlock control shall comply with the principles defined in the Guidelines for the Design of the Plant Interlock System [RD11], in particular with respect to determinism, segregation from conventional control, and avoidance of common-cause failures. Logical and, where required, physical separation from conventional control shall be ensured whenever necessary to preserve the integrity and availability of protection functions.

7.9.5.1.2   Interlock functions

Interlock functions shall be implemented in a manner consistent with their assigned Investment Protection Integrity Levels (3IL) as defined through the process governed by the ITER Investment Protection Handbook [AD48]. The interlock control shall ensure that protective actions remain effective under all fault conditions and are not inhibited or degraded by failures in conventional control or plant communication systems.

7.9.5.1.3   Configuration and integration

The configuration and integration of the VS3-PS PIS into the ITER interlock environment shall comply with the Guidelines for PIS configuration and integration [RD12]. This includes, in particular, requirements related to signal modelling, configuration consistency, naming

conventions, and integration testing within the CIS framework. The design shall allow coherent integration into ITER's global interlock configuration and support controlled evolution over the project lifetime.

7.9.5.1.4 Parameterisation

The interlock control shall support a controlled degree of parameterisation of interlock functions, as specified in Section 6.4, under CIS governance. Such parameterisation shall ensure traceability, access control and configuration coherence at plant level. Local or conventional control systems shall not modify interlock parameters autonomously.

7.9.5.1.5 Precedence

Interlock actions shall always prevail over conventional control in case of conflict. The design shall ensure that failures of communication or control subsystems do not prevent the execution of local protective actions. Where required by the protection objectives, interlock actions shall be implemented through dedicated or deterministic paths, independently of non-deterministic plant networks.

7.9.5.2 *High Integrity Interlocks (3IL-3/SIL-3)*

For the implementation of High Integrity Interlocks (3IL-3/SIL-3), the design, configuration and integration of the interlock controller shall strictly apply the

1. Guidelines for the Design of the Plant Interlock System (PIS) [RD11], and the
2. Guidelines for PIS configuration and integration [RD12].

7.9.5.3 *Implementation – hardware selection*

The technical implementation of the interlock control shall rely on ITER-approved hardware and I&C components selected from the applicable ITER hardware catalogues. The use of qualified and catalogued PLCs, I/O modules, communication interfaces and safety-related components is mandatory unless otherwise explicitly approved by IO.

The DA shall ensure that all hardware components used for interlock control are compatible with the assigned integrity levels and with the environmental, EMC and seismic constraints applicable to VS3-PS.

The DA shall further ensure that the selected hardware supports the integration and configuration constraints imposed by [RD11] and [RD12], including compatibility with CIS interfaces, time determinism where required, and long-term maintainability within the ITER I&C ecosystem.

In particular, the main interlock controller(s) shall be selected from:

- ITER catalogue for I&C products - Slow controllers PLC [RD23],
- Catalogue for I&C products – Fast controllers [RD24]

7.10 Main Steel Structure

The Main Steel Structure is a two-storey structure that houses all VS3 Power Supply System equipment. A conceptual illustration is provided in Figure 7-6.
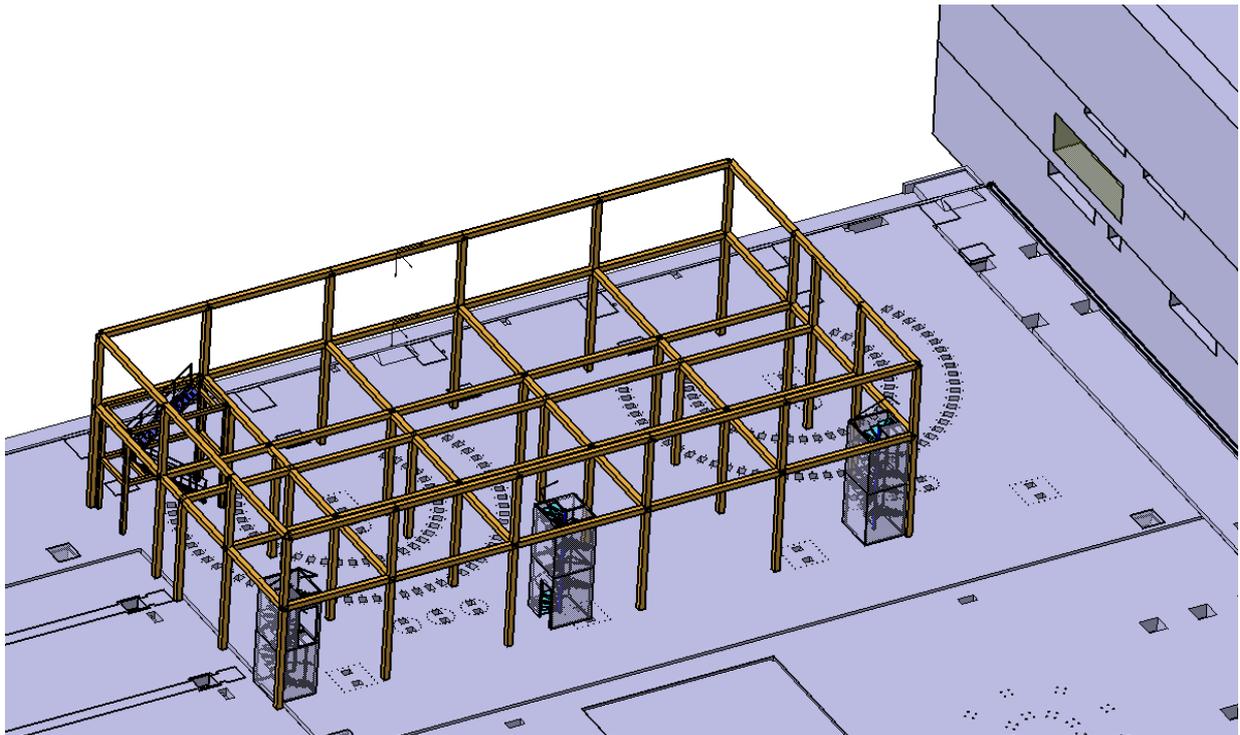
Figure 7-6: concept of main steel structure in B13 (from VS3-PS CDR)

7.10.1 Arrangement requirements

The main steel structure shall occupy the entire footprint reserved for the VS3-PS system in B13 [AD89].

The ground level (starting from level L1) shall be dedicated to inter alia the following components:
1. I&C and LV Distribution panels and cubicles
2. …

The ground level area will be classified as "electrical area" as per NF C 18-510 [CS26] and will require specific accreditations for workers to access it.

The first floor shall be dedicated to inter alia the following components:
1. Energy Storage Capacitor Bank modules
2. …

The first-floor area will be classified as "electrical area" as per NF C 18-510 [CS26] and will require specific accreditations for workers to access it.

The following areas are classified as "Independent Access Areas":
1. MV Switchgear area
2. I&C and LV cubicles/panels area

Independent access means that each access shall be individually controlled by physical means. Uncontrolled crossing from one (sub-)area to another is not allowed.

Access rules including the physical implementations (e.g. number and positions of doors) for electrical areas are to be defined based on applicable standards. The guidelines and requirements for safe access, circulation space, staircases, etc. described in [AD73] shall be taken into account. Provisions shall be included to allow the posterior possible implementation of an access control system by IO.

All subareas shall be equipped with lights, electrical sockets and other services in accordance with the relevant standards.

The main steel structure shall be designed in such a way that externally interfaced systems can access the VS3-PS components with which interfaces are required.

Not all physical interfaces (e.g. SSEN, CODAC, CIS, etc.) have been defined in full detail yet. However, these interfaces will be routed to the interface points located inside the main steel structure with cables trays in accordance with the boundaries and responsibilities specified in section 9.9.

7.10.2 Design requirements

The requirements in this section apply to the primary and secondary steelwork of the main steel structure. A primary structure is understood as a member of the backbone of the VS3-PS main steel structure, for instance the vertical columns of the main steel structure attached to the anchor plates. A secondary structure is understood as an internal member of the backbone of the main steel structure.

The primary and secondary steelwork include the components listed in Table 7-2.

Table 7-2: description of primary and secondary steelwork

Primary steelwork	Secondary steelwork
Floor beams	Structural steel stairs
Columns	Flights and landings
Plan bracing members	Handrails
Inclined cantilever props	Balustrades
	Durbar plating
	Open Mesh Flooring

The design of the VS3-PS Main Steel Structure in B13 shall be in accordance with Eurocode including the French National Annexes, as per section 8.7.2.

The main steel structure shall be designed considering the internal and external loads defined in the load specification in reference [AD38].

The design of the main steel structure shall equally take into account the interface requirements with PBS 44 listed in section 9.9.2.

The raw material of the main steel structure shall be procured based on the standards listed in Table 7-3 or equivalent.

Table 7-3: codes and standards for procurement of raw materials for main steel structure

Type of beam	Carbon steel		Stainless steel	
	Grade	Standards	Grade	Standards
Opened section	S355	EN 10025-2	1.4404	EN 10088-5
Hollow square		EN 10210-1		
L-angle		NF EN 10056-1		
Plates		EN 10025-2		EN 10088-4

A margin of 20 % shall be considered on the masses of the VS3-PS system components that are supported by the main steel structure. This requirement is motivated by the need to anticipate future VS3-PS system updates or new equipment to be implemented during the lifetime of the VS3-PS system. In case this margin is too impactful, a deviation may be granted in duly justified cases.

All floors shall be implemented with non-perforated gratings. All gratings shall be anti-slip. These requirements also apply to the staircases.

The areas not directly supporting VS3-PS components and devoted to circulation (grating, staircases…) shall be designed to support a live load of 500 daN/m^2.

The size of the openings of the meshing of the grating shall be such that a ball with a diameter of 20 mm cannot fall through according to reference ISO 14122-2

The necessary iterations of the design shall be performed to achieve the acceptance criteria and to optimize the material, beams sizing and shapes. These iterations shall be calculated based on elastic analyses when subjected to various combinations of loads such as dead, live, thermal, seismic, magnetic, fire, accidental and defined loads combination.

7.10.3 Material requirements

The material used for the main steel structure shall be S355 EN 10210 carbon steel or stainless steel (or equivalent).

The choice of material shall consider the Static Magnetic Field effects on the main steel structure (if any).

If carbon steel is used, the coating requirements defined in section 8.10.3 shall be considered.

7.10.4 Fasteners requirements

For all bolted connections between members of the backbone of the main steel structure (primary structures), the fasteners should have a minimum diameter of 20 mm unless justified otherwise.

For all secondary structures, the fasteners should have a minimum diameter of 16 mm unless justified otherwise.

For bolted or clamped connections in all primary structures, at least 4 bolts shall be implemented at each attachment or clamping point, unless justified otherwise.

For connections in all the secondary structures, at least 2 bolts shall be implemented.

The Minimum grade of bolts should be 8.8.

Punching of bolt holes is not allowed.

Unless duly justified, the bolts used for fastening components subjected to vibration or significant load variation shall be secured with Split pins in reference NF EN ISO 1234 or equivalent.

7.10.5   Execution requirements

The execution of the steelwork shall follow EN 1090 [CS39].

8 System-Level Technical Requirements

8.1 Insulation Coordination

Upstream the primary winding of the transformer(s) of the VS3-PS rectifiers, the insulation coordination of the VS3-PS system shall be compliant with the NF C 13-200 [CS24] and IEC 60071-1 [CS5] standards. Isolation levels are defined in IEC 60071-1, whereas NF C 13-200 defines some related requirements such as isolation distance, etc.

Downstream the secondary winding of the transformer(s) of the VS3-PS rectifiers, the insulation coordination of the VS3-PS system shall be compliant with the IEC 60664 [AD6] standard. The overvoltage category shall be Category II or better, unless the DA demonstrates that other categories can equivalently be considered.

Irrespective of the referenced standards on insulation coordination, it shall be possible with reasonable efforts to conduct dielectric tests on the VS3 Extension Busbars, VS3-related IVC Busbars and VS-coils with the following voltage levels, simply by opening the output disconnectors of the VS3-PS:

1. DC voltage of up to 2.7 kVdc, permanent
2. AC voltage of up to 6.4 kVac at 50 Hz for 1 minute

Reasonable efforts may comprise the removal of a limited number of components such as transient voltage limiting devices, voltage and current sensors, etc.

8.2 Earthing

The ITER EDH Part 5: Earthing and lightning protection [AD16] provides details on the ITER site integrated earthing grid and the earthing methodology to be followed for the earthing of all plant systems components used or installed at ITER project.

In addition, this document includes the rules for the lightning protection system for ITER buildings.

Specific earthing requirements are provided, where applicable, within the subsystem technical requirements (chapter 7).

8.3 General Component Requirements

8.3.1 Capacitors

8.3.1.1 Energy Storage Bank Capacitors

For the Energy Storage Capacitor Bank cells, only dry-type Metallized Polypropylene (MPP) capacitors shall be deployed.

8.3.1.2 Power circuit capacitors

For all capacitors implemented in the power circuit, dry type capacitors shall be used.

8.3.1.3 Electrolytic Capacitors

The use of electrolytic capacitors shall be avoided unless strictly required, in order to permit prolonged periods of storage and non-operating conditions.

8.3.2 Inductors & Transformers

The power inductors and power transformers shall be dry type, with fire behaviour class F1 or F2.

8.3.3 Power electronic switches

8.3.3.1 Harmonization of semiconductor switch devices

Identical semiconductor switches and associated gate-driver units shall be employed in the rectifier and inverter stages of both power converters, for the purpose of standardizing procurement and simplifying spare-parts management.

8.3.3.2 Parallel switches and switch modules

8.3.3.2.1 Minimization of current imbalance

All possible and reasonable efforts shall be taken to minimize the static and dynamic current imbalance between parallel semiconductor switches. Such efforts may include equalisation of parasitic elements in the power and gate drive circuits, homogenizing the thermal conditions (thermal resistance, heat sink temperature, etc.), selecting and sorting devices based on measured device characteristics (Vce(sat), Vth, etc), grouping by manufacturing batch, etc.

Each semiconductor switch shall have a dedicated gate driver.

8.3.3.2.2 Current imbalance limits

With reference to the definitions of Figure 7-2, the static current imbalance between different inverter/rectifier modules shall be limited to 15%, whereas the current imbalance between different switch modules part of the same inverter/module during the on-state (conduction) shall be limited to 20%. The current imbalance is defined as the difference between the highest and lowest switch conduction current, over the arithmetic mean switch conduction current.

8.3.3.3 Junction temperature

The virtual junction temperature of the semiconductor switches shall be at least 15 °C below the nominal operating temperature stated in the component datasheet. This requirement applies for normal operation of the power converters, under nominal conditions of power, voltage, current, ambient and cooling water temperature, etc.

Under fault conditions, the junction temperature shall conform to the recommendations of the device manufacturer or to the applicable standards.

The virtual junction temperature shall be considered in accordance with IEC 60747-9 [CS3].

8.3.3.4 Thermal cycling

For this pulsed application, the junction temperature variation (ΔTj) is significant and the number of thermal cycles is high. The thermal cycling capacity of the power electronics switches is an

important design aspect. The DA shall demonstrate that their design complies with the required thermal cycling profile and is compatible with the required service life.

8.3.3.5 Overtemperature monitoring

Overtemperature monitoring shall be implemented on each switch module of the inverters and rectifiers. The overtemperature monitoring at switch-module level shall contribute to the overall overtemperature interlock function (see section 6.4.3.6). Temperature sensors or temperature switches may be employed for this purpose. Although overtemperature conditions shall be monitored on every switch module, only the aggregate switch module overtemperature status of each inverter and each rectifier needs to be reported; accordingly, a series-connection of thermal switches is acceptable.

8.3.3.6 Cooling

All power electronic switch modules shall be water cooled.

8.3.4 Voltage and current sensors

8.3.4.1 Hall-effect sensors

Where Hall-effect sensors are employed, careful consideration shall be given to remanent magnetism resulting from current peaks near or exceeding the full-scale rating. If the occurrence of such current peaks cannot be excluded and the use of Hall-effect sensors is unavoidable, the selection of the sensor shall be adapted accordingly, or the necessary compensation mechanisms or demagnetization circuits shall be implemented.

8.4 Power circuit system design

The power circuit of the VS3 Power supply shall be designed and dimensioned in consideration of the pulsed power application corresponding to its use.

8.4.1 Internal impedance

The internal impedance of the power converters shall be designed and controlled so to not significantly affect the power supply performance, i.e. the voltage drops across conductors and components need to be limited accordingly.

Internal impedances of the power converter typically comprise the series resistances and stray inductances of cables, busbars, capacitors, fuses, filters, semiconductor switches, etc.

Cables in the power circuit shall be dimensioned based on the maximum allowable voltage drop for the pulsed power application, and not solely for thermal constraints.

In addition, stray inductances shall be minimized through design to suppress system oscillations, particularly for circuits and components (such as capacitors) around the semiconductor switches.

8.5 Enclosures, Cabinets and Physical Arrangement

The design of the enclosures and cabinets shall enable rapid and straightforward installation and removal of the power supply within the allocated space.

8.5.1 Modular architecture

The physical realisation of VS3-PS shall be based on a modular design to facilitate installation, commissioning, maintenance and spare-parts management.

The physical subdivision of the power supply into modules shall be based on functional partitioning, with dedicated modules assigned to the rectifier, inverter, ESCB, control hardware, and other main subsystems. Large subsystems such as the inverter and the ESCB shall be implemented as assemblies comprising multiple modular enclosures as required.

Each module shall be identical to all other modules fulfilling the same function.

8.5.1.1 Independence and standalone operation

Modules shall be designed as much as reasonably possible to permit standalone operation, i.e. each module should be capable of performing its primary functions upon connection of the required utilities and control signals, without dependence on components or services provided by other modules. For example, inverter modules shall incorporate sufficient onboard DC-side capacitance onboard to enable meaningful testing.

8.5.1.2 Regulatory inspections and acceptance testing

The subdivision into and design of the modules shall specifically consider the possibility of standalone operation to enable inspections and testing at the module level.

The modular architecture and interconnections shall allow for a sequential inspection and verification process, whereby each module undergoes regulatory assessment individually prior to integration into the complete system, for the purpose of reducing the risk of delays before and during final assembly and commissioning.

8.5.1.3 Electrical integrity and safety provisions

All necessary electrical integrity and safety provisions shall be implemented at the module level to guarantee that each physical module remains safe during transport, storage, and post-energization activities, including testing. This may include local earthing switches, bleeder resistors, Electrostatic Discharge (ESD) protections, signal-line terminations, etc. Where required, such provisions shall be operable from outside the enclosure.

8.5.1.4 Connectivity

The power supply modular enclosures shall allow for rapid connection and disconnection of all low-voltage and data communication interfaces, for which fast connectors may be considered.

For I&C and data communication interfaces, the use of multi-fibre connectors for inter-module links and for connections to central I&C systems shall be considered.

All exposed conductors and connectors shall be equipped with protective covers for use during storage and transport.

8.5.2   Disposition

The general arrangement and internal layout of the modules shall, among other factors, be defined in accordance with the requirement to minimise loop impedance of the power circuit (see section 8.4.1).

The location of the interface points with the required services shall be taken into account in the disposition of the modules such that the length of interfacing cables, fibres and piping remains within reasonable limits and without adverse effects on performance.

The general arrangement shall also account for installation and maintenance constraints; replacement of a power supply module within the VS3-PS allocated space shall be achievable with reasonable effort.

8.5.3   Subsystem enclosures

The selection and/or design of the enclosures of the modules shall be performed by the DA.

The use of shipping containers as enclosure for the ESCB modules and potentially other power supply modules may be considered.

8.5.3.1   Structural resistance

All enclosures shall be selected and/or designed to prevent any plastic deformation of structural elements resulting from pressure waves (blasts) generated by electrical faults, particularly those directly or indirectly associated with the ESCB. The enclosures of the ESCB shall, in addition, the comply with all requirements specified in section 7.3.4.

8.5.3.2   Degree of protection (IP)

All subsystems or components that contain electrical and/or electronics parts shall be enclosed with the following minimal degrees:

a.   IP degree: IP30 as per IEC 60529 [CS19]

b.   IK degree: IK07 as per the IEC 62262 [CS20]

8.5.4   I&C Cubicles

The control system cabinets (controller, signal conditioning …) shall be selected and implemented as per:

1. ITER catalogue for I&C products – Cubicles [RD22]
2. I&C cubicle internal configuration [RD25]

8.6 Cables and Cable Trays

This section provides general requirements applicable to internal cable trays (including conduits) and cables that are implemented in the VS3-PS system.

The cables and cables trays shall be selected and installed following the requirements listed in the following documents:
- IO cabling rules [AD19]
- IO cable catalogue [AD20]

8.6.1 Cables

The type of conductors (busbar, cables, braids, etc.) and all relevant ratings for all internal connections, as well as for all connections with externally interfaced system (VS3 extension busbars, SSEN, PPEN, etc), shall be defined by DA.

The cable dimensioning for the power circuit shall take into account the requirements specified in section 8.4.

8.6.2 Cable trays

All cables shall be routed in non-perforated metallic trays. The corresponding reaction to fire classification shall satisfy the INB requirements with a minimum class of C1 based on reference NF C 32070 and the equivalent Euroclass Cca-s1b-d1a1 according to EN50575 and additionally IEC 60754-1.

All cables shall be attached to the cable trays with the appropriate cable ties. These cable ties shall be located every 1.5 m or at any direction change or exit of cables from the tray.

All cables placed inside of a solid bottom tray shall be also attached together with cable ties.

The size of cable trays shall be selected in consistency with the defined sizes in [AD19].

The number of different cable trays sizes shall be limited.

For each cable tray, the filling rate shall not exceed 50 % unless duly justified.

The design of the cable trays and their supports shall take into account the VS3-PS load specification [AD38], and all additional specific load specifications documents produced.

The supports shall be able to support the full load capability of the cable trays.

The cable trays shall be hot-dipped galvanized after fabrication.

The thicknesses of ladder and solid bottom trays shall be 1.5 mm (excluding covers and accessories).

The design, material, construction, manufacturing, inspection, testing and performance of all cable products supplied shall comply with currently applicable standards, regulations and safety codes in France.

8.7 Structural Requirements

This section applies to steel frames of the internal components of the VS3-PS fixed on the main steel structure, for instance the frames of the electrical cubicles or any mechanical component or equipment fixed on the VS3-PS main steel structure.

This section applies to components designed by the DA.

This section does not apply to non-customized, standard finished components procured on the market (Commercial Off The Shelf products).

The DA is responsible to make sure COTS components meet the resistance requirements specified in this document and in the load specifications in reference [AD38].

8.7.1 General safety rules for structural components

The VS3-PS system is classified SC2. All the components shall be designed in such a way that they never damage other systems around.

The structural frames of all internal components or all cabinets of the VS3-PS shall be designed to withstand the loads provided in the load specification [AD38] and all specific load specifications documents produced additionally.

The frames, their fixation devices and the welds shall remain stable under the load combinations provided in the load specification [AD38].

A minimum margin of 30 % should be targeted on the result of each load combinations during the structural analysis.

Notes:

(1) This requirement is motivated by the need to anticipate future VS3-PS system updates or new equipment to be implemented during the lifetime of the VS3-PS system.
(2) If this margin is too impacting, a deviation may be possible based on strong justifications.

8.7.2 Design code

All structural components shall be designed in accordance with the Eurocodes, including the French National Annexes. The applicable codes include but are not limited to:

- Eurocode 0 (EN 1990),
- Eurocode 1 (EN 1991),
- Eurocode 3 (EN 1993), and
- Eurocode 8 (EN 1998).

For design according to Eurocodes, the following documents shall be considered:

a. ITER Structural Design Code for Buildings (I-SDCB) - Part1: Design Criteria [AD92]
b. ITER Structural Design Code for Buildings (I-SDCB) - Part 2: Construction [AD93]

For structural components that do not ensure the safety of people, the design may also be based on the ANSI/AISC 360 [CS38] calculation code.

Structural components not ensuring the safety of people include, but are not limited to, mechanical supports of electrical components, pipes supports or frames of electrical cabinets, etc.

Structural components ensuring the safety of people include, but are not limited to, the VS3-PS Main Steel Structure in B13, overhead structures, stairs cages, bridges, etc. (their collapse could injure persons).

8.7.3   Fixation of the VS3-PS internal components

8.7.3.1.1   For components fixed on the main steel structure

For the fixation of VS3-PS components on the VS3-PS main steel structure in B13, several fixation solutions are possible, including welding. The DA shall select the type of fixation based on the geometry of the components being assembled.

The DA shall make sure that the fixation solution permits the dismounting of the system.

8.7.3.2   *For the components fixed on the B13 slab*

For the fixation of components on the B13 slab, the procedure described in section 9.11.2 applies.

8.7.4   Execution requirements

The execution of the steelwork shall follow EN 1090 [CS39].

8.7.5   Material of structural parts of the internal components of the VS3-PS

For the material of structural parts of the internal components of the VS3-PS it is suggested to use the material in table below.

Table 8-1: material of structural parts of the internal components

Type of beam	Carbon steel		Stainless steel	
	Grade	Standards	Grade	Standards
Opened section	S355 S235	EN 10025-2	1.4404	EN 10088-5
Hollow square		EN 10210-1		
L-angle		NF EN 10056-1		
Plates		EN 10025-2		EN 10088-4

If the DA decides to use another material, they shall make sure the material complies with the requirement on materials and with the electromagnetic compatibility.

8.8   Piping Requirements

The design and implementation of all pipes and cooling water networks shall be in accordance with the Pressure Equipment Directive (PED) [CS31].

The pipes and cooling water networks shall be designed considering the requirements specified in the PED on the maximum allowable pressure, plus an additional margin of 10 % for fluctuation. For all piping and cooling water network parts that are exposed to PBS 26.CC.2A

pressure levels, the design pressure is imposed as interface requirement and the additional margin should be considered as already included.

In case water-to-water heat exchangers are used, the design pressure on the secondary side downstream the exchanger shall equally be defined in accordance with the PED [CS31].

8.8.1 Design codes

The codes defined in Table 8-2 shall be considered for the design of the piping system. Either ASME or EN codes according to [RD29].

Table 8-2: design codes applicable to the design of VS3-PS cooling water networks

Design of pipes and their supports	EN 13480-3
	ASME B31-3
Pipe dimension	EN 10216-5
	ASME B36.19
Design of fittings	EN 10253-4
	ASME B16.5
	ASME B16.9

The following documents shall be produced as part of the design deliverables:
   a) Pipe stress analysis calculation methodology document
   b) Hypothesis note for pipe stress analysis
   c) Piping class document
   d) Piping class validation document

A pipe stress analysis shall be performed on the piping system in accordance with [RD29].

8.8.2 Materials

All metallic parts in direct contact with the water of the PBS 26.CC.2A cooling water network shall be made of copper or stainless steel and be compatible with the existing pipes at the interface point.

If stainless steel is used, the characteristics shall comply with the material requirements in Table 9-4 (or equivalent).

Irrespective of the material, the requirements in section 8.10.1 shall be considered.

8.8.3 Supports

The supports of pipes shall be designed in such a way to limit the deflection of pipes to L/500 where L is the pipe span of the supports calculated by DA. The calculated span also applies between the last support of PBS 26 and the first support of VS3-PS.

The pipe supports may be constructed from carbon steel or stainless steel. In case carbon steel is used, the requirements defined in section 8.9.1 shall be considered. In case stainless steel is used, the material specification in Table 9-4 shall be implemented.

8.9   Auxiliary Power

This section specifies the system-level requirements on the supply of auxiliary power to VS3-PS components. Specific requirements concerning the interface with the supply network (SSEN) are provided in section 9.8.

8.9.1   Class II-IP supply – Investment Protection Loads

All Systems, Structures and Components involved in protection functions shall be powered by the SSEN Class II-IP supply network.

In all cubicles housing Investment Protection I&C equipment, both Class II-IP and Class-IV supply shall be provided.

8.9.2   Class II-IP supply – Power Supply Loads

In addition, all critical and sensitive components of the power supply shall be fed by Class II-IP supply, including but not limited to the following component types:

- I&C – sensors, controllers, signal conditioning, media converters, etc.
- Gate drivers, electronic assemblies, interface boards, etc.
- Circuit breakers, differential protection, transformer protection, overtemperature protection, etc. (monitoring, control and actuators)

The components powered by SSEN II-IP shall further comprise all those necessary for maintaining communication with ITER's control networks and for the VS3-PS remaining operational as per the provisions in section 6.8.

8.9.3   Class IV supply – Ordinary Loads

All other, ordinary loads shall be powered by the SSEN Class IV-OL network. Such loads may comprise heat exchanger fans, pumps, large actuators, etc.

8.9.4   Local UPS

The use of local Uninterruptible Power Supply (UPS) devices shall be avoided. Auxiliary components requiring uninterruptible power supply shall be supplied from the corresponding SSEN networks. Local UPS devices may be considered only in duly justified cases and shall be subject to IO's prior acceptance, supported by a comprehensive operation and maintenance plan.

8.10 Materials

8.10.1 General requirements

All materials, coatings, insulation and paint shall be free of halogens.

8.10.2 Impurities

No impurity limits apply to austenitic stainless-steel materials in Building 13.

8.10.3 Coating requirements

In B13, the coating service level III (or equivalent) shall be applied to the VS3-PS system components, in accordance with ASTM D5144 [CS37].

For carbon steel, it is suggested to use galvanization according to section 8.10.3.2.

For other materials, the necessity of coating shall be defined based on existing standards, experience or industrial best practices.

8.10.3.1 Requirements for painting

The following standards (or equivalent) shall be considered when implementing the paint:

- EN 12944-1: Corrosion protection of steel structures by protective paint systems - Part 1: General introduction
- EN 12944-2 (C2): Corrosion protection of steel structures by protective paint systems - Part 2: Classification of environments
- EN 12944-4: Corrosion protection of steel structures by protective paint systems - Part 4: Types of surfaces and surface preparation
- EN 12944-5: Corrosion protection of steel structures by protective paint systems- Part 5: Protective paint systems (A2.07)

8.10.3.2 Requirements for galvanization

Galvanization shall comply with EN ISO 1461 [CS41] (or equivalent).

8.10.3.3 On-site repair of coatings

For on-site repair of damaged coatings, the preparation of substrates before application of paints and related products shall be in accordance with EN ISO 8501 [CS42].

9 Interfaces and Interface Requirements

9.1 Interface Management

The identification of interfaces, the definition of interface requirements, the development of interface solutions, and the control of the related interface documentation shall be performed in accordance with the Design Interface Control Procedure [AD33].

9.1.1 Interface definition

The definition of all major interfaces, as well as changes to existing interface definitions captured in the applicable Interface Sheets, shall be completed and frozen by the conclusion of the Preliminary Design Review phase.

9.1.2 Interface document responsibilities

Table 9-1 summarises the applicability and update responsibilities in regard to interface documents.

The applicability, Reference Document or Applicable Document, is to be understood in accordance with the definitions in section 4.1.

Whereas the responsibilities are already defined, the ultimate need of the currently not created interface documents marked with an asterisk (*) is to be confirmed during the execution of the Task Agreement.

Table 9-1: applicability and update responsibilities in regard to interface documents

#	Title	UID	Applic ability	Responsible for update
1	Interface Control Document (ICD) between Coil Power Supply and Distribution (PBS 41) and In-Vessel Coils (PBS 15-IV)	ITER_D_3MSYPA	-	IO
2	Interface Control Document (ICD) between Plant Installation Tooling (PBS-22) and Coil Supply & Distribution (PBS-41)	ITER_D_33ACF8	AD	IO
3	Interface Control Document (ICD) between Component Cooling Water System (PBS-26CC) and Coil Power Supply & Distribution System (PBS-41)	ITER_D_2FPYX7	AD	IO
4	Interface Control Document between PPEN (PBS41.PP) and AC/DC Converters (PBS41.xx)	ITER_D_2KSK3W	RD	IO
5	ICD-41-43 Interface Control Document for Steady State Electrical Network (PBS 43) and Coil Power Supply and PPEN (PBS 41)	ITER_D_35BQZA	AD	IO
6	Interface Control Document between Coil Power Supply and Distribution (PBS 41) and Cable Tray Systems (PBS 44)	ITER_D_CGQ4PD	AD	IO
7	ICD-41-45 Interface Control Document for Coil Power Supply & Distribution (PBS 41) and CODAC (PBS 45)	ITER_D_2NKSW9	AD	IO
8	ICD-41-46 Interface Control Document for Coil PS & Distribution (PBS 41) and Central Interlock System (PBS 46)	ITER_D_2M58GX	AD	IO
9	ICD-41-47 Interface Control Document for for Plasma Control System (PBS 47) and Coil Power Supplies & Distribution (PBS 41)	ITER_D_33KFL9	AD	IO
10	Interface Control Document (ICD) between Coil Power Supply and Distribution (PBS41) and Assembly Building (PBS62.13)	ITER_D_9MPWW6	AD	IO
11	IS-15.IV-41-001	ITER_D_JK87TY	-	IO
12	IS-22-41-003	ITER_D_5XL6W4	RD	IO
13	IS-26.CC.2A-41-001 Interface between PBS26.CC.2A and Coil Power Supply & Distribution (PBS 41)	ITER_D_DABD6D	AD	IO
14	IS-41PPAJ-41_IVCPowerSupplies-001	ITER_D_DY6EG9	RD	IO
15	IS-41-41-003 Interface Sheet between VS3 Power Supply (41.V3) and VS3 Busbars (41.V3.BB / 41.V3.BE)	ITER_D_FG5WSV	AD	IO
16	IS-43-41-501 Interface between LV Class IV Power Supply of SSEN and In-vessel coil power supply	ITER_D_M2WS9P	AD	IO
17	IS-43-41-502 Interface between Class II-IP Power Supply of SSEN (PBS 43.BR) and In-vessel coil power supply (PBS 41.EL/V3)	ITER_D_E2ZJZF	AD	IO
18	IS-41.V3-44-001 Interface sheet between VS3 Power Supply (PBS 41.V3) and Cable Tray System (PBS 44)	ITER_D_ELVTJ7	RD	IO
19	IS-41-45-008 – Interface between V3PS and CODAC	ITER_D_CCSGVS	AD	IO
20	IDS-41-45-00x - Interface Data Sheet between V3PS Plant System I&C of PBS 41 and PBS 45	TBD	-	DA
21	IS-41-46-009 – Interface Sheet (IS) between V3PS Plant Interlock System of PBS41 and PBS46	ITER_D_CD899M	AD	IO
22	IDS-41-46-009 - Interface Data Sheet between V3PS Plant System of PBS41 and PBS 46	TBD	-	DA
23	IS-47-41-005 Interface Sheet between PBS47 (PCS) and PBS 41 (CPSS – VS3) – Architecture	ITER_D_7PE9R4	AD	IO
24	IS-47-41-006 Interface Sheet between PBS47 (PCS) and PBS 41 (CPSS – VS3) – Requirements	ITER_D_7PEA3L	AD	DA
25	IS-41-62.13-001 Interface sheet between PBS41.EL, PBS41.V3 and PBS62.13	ITER_D_9RCYJ5	AD	IO

9.2 Vertical Stabilization coils (VS Coils, PBS 15.IV)

The VS3 Power Supply has a functional interface with the VS coils of PBS 15.IV: it provides controlled voltage/current to the coils.

There is no direct physical interface between the VS coils and the VS3 Power Supply in scope of this Technical Specification. The physical interface point between both systems lies at the end of the feedthroughs of PBS 15.IV, as illustrated in Figure 9-1. The IVC busbars extend the feeders to the VS3 Linkboard at Building 11-L4 (both 41.V3.BB), where the series and anti-series connections of the coil turns are made. The VS3 Extension Busbars (41.V3.BE) finally connect the VS3 Linkboard to the connection box in the VS3-PS area in Building 13, where the interface between the VS3 Power Supply (41.V3) and the VS3 Extension Busbars (41.V3.BE) is physically located.
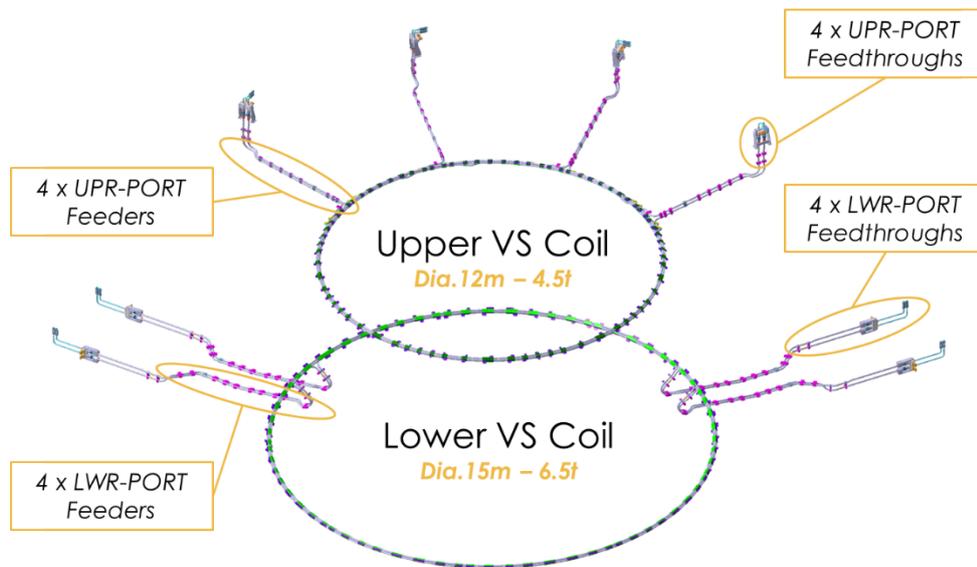

Figure 9-1: representation of VS-coils (VS3), comprising two anti-series connected coils of 4 coil turns each. The interface with PBS 41.V3 lies at the end of the feedthroughs.

9.2.1 Coil turn configuration

In normal operation, four turns of the upper VS3U coil and four turns of the lower VS3L coil are connected in series, with the two coils being connected in an anti-series arrangement. In case of failure of any of the 8 turns, the defective turn will be isolated from the VS3 coil circuit by means of the VS3 Linkboard.

In order to maintain symmetry between the upper and lower coil, a healthy turn on the opposite coil is equally taken out of service. The resulting 6-turn coil circuit needs to be operated by VS3 Power Supply with the same Ampere-turns, resulting in an operating current that is (4/3) times the nominally rated (8-turn) current level. The VS3 Power Supply thus needs to be capable of delivering higher output current and be capable of accommodating the (offline) change in load impedance.

The performance requirements for both 6-turn and 8-turn operation are listed in the corresponding section 6.1.

9.2.2   Admissible current and voltage levels

9.2.2.1   Admissible current levels

The VS3 Power Supply shall be designed to ensure that the maximum admissible current levels defined for the PBS 15.IV coils, feeders and feedthroughs are not exceeded under any operating condition including any possible fault scenario. The limits defined by PBS 15.IV are provided in Table 9-2. Both instantaneous and thermal limits shall be strictly respected.

In particular, the maximum instantaneous current in the VS3 coil circuit shall be strictly limited to 95 kA in the framework of nuclear safety (refer to section 12.2), and to 90 kA in the framework of investment protection.

Table 9-2: admissible current levels defined by PBS 15.IV for the VS coils, VS coil feeders and feedthroughs. The stated load categories refer to those defined in

	Safety	Investment Protection
	Feedthroughs (15.IV)	VS coils & feeders (15.IV)
6-turn (faulted) configuration		
Maximum peak (instantaneous)	95.4 kA	75 kA Cat I/II 90 kA Cat III
Maximum I^2*t (thermal) (400s plasma scenarios)	$1.44 \cdot 10^{12}$ A$^2 \cdot$s ***	$1.44 \cdot 10^{12}$ A$^2 \cdot$s *
Maximum continuous rms (400s plasma scenarios)	4 kA -> ITER Entire Life Cycle 4-60 kA -> reduction in duration due to fatigue***	4 kA -> ITER Entire Life Cycle 4-60 kA -> reduction in duration due to fatigue**
8-turn configuration		
Maximum peak (instantaneous)	95.4 kA	75 Cat I/II 90 Cat III
Maximum I^2*t (thermal) (400s plasma scenarios)	$1.44 \cdot 10^{12}$ A$^2 \cdot$s ***	$1.44 \cdot 10^{12}$ A$^2 \cdot$s*
Maximum continuous rms (400s plasma scenarios)	4 kA -> ITER Entire Life Cycle 4-60 kA -> reduction in duration due to fatigue***	4 kA -> ITER Entire Life Cycle 4-60 kA -> reduction in duration due to fatigue**

* Considered enveloped by Maximum continuous rms and Operation currents requirements, I^2*t calculated as I=60 kA and t=400s

** Increase in rms current poses no risk for thermal aspect, but will decrease number of operation cycles due to higher fatigue on components.

*** VS FTs considered enveloped by VS Coils as they can handle higher current.

9.2.2.2   Admissible voltage levels

The voltage between the inner conductor and outer casing of each VS coil, feeder and feedthrough shall not exceed 2.4 kV under any operating condition including transients, resonances, etc. For normal operation, disregarding switching transients, this requirement is enveloped by the power supply maximum output voltage.

For information, the VS3 coils insulation has been designed for a testing voltage of 5.8 kVdc (1.7 kVac RMS).

9.2.2.3 Output voltage slew-rate

The voltage slew-rate (dV/dt) at the interface point between PBS 15.IV.VS and PBS 41.V3 shall not exceed 175V/us. This requirement is enveloped by the overall power supply output slew-rate limitation (refer to 7.5.3), which is considerably lower.

9.2.3 Electrical impedance

The electrical impedance of the VS coils (in 8-turn configuration) and the feeders up to the end of the feedthroughs is provided in "IVC impedance" [RD44]. The calculated impedance includes the effect of inductive coupling with the surrounding passive structures. Stray capacitance, predominantly between the conductors and the earthed outer casings, is not integrated into the results. The accuracy of the reported resistance and inductance is decreasing from 50 Hz onwards, due to assumptions and simplifications, such as on the blanket modules.

The self-inductance and resistance at DC of the VS coils and their feeders is given in Table 9-3. The equivalent series inductance and resistance over frequency are provided in Figure 9-2.

Table 9-3: self-inductance and resistance at DC of VS-coils and their feeders, at 100°C [RD44].

	VS3 coils + feeders	
	R (mΩ)	L (mH)
8-Turn	14.0	1.33
6-Turn	10.5	0.783

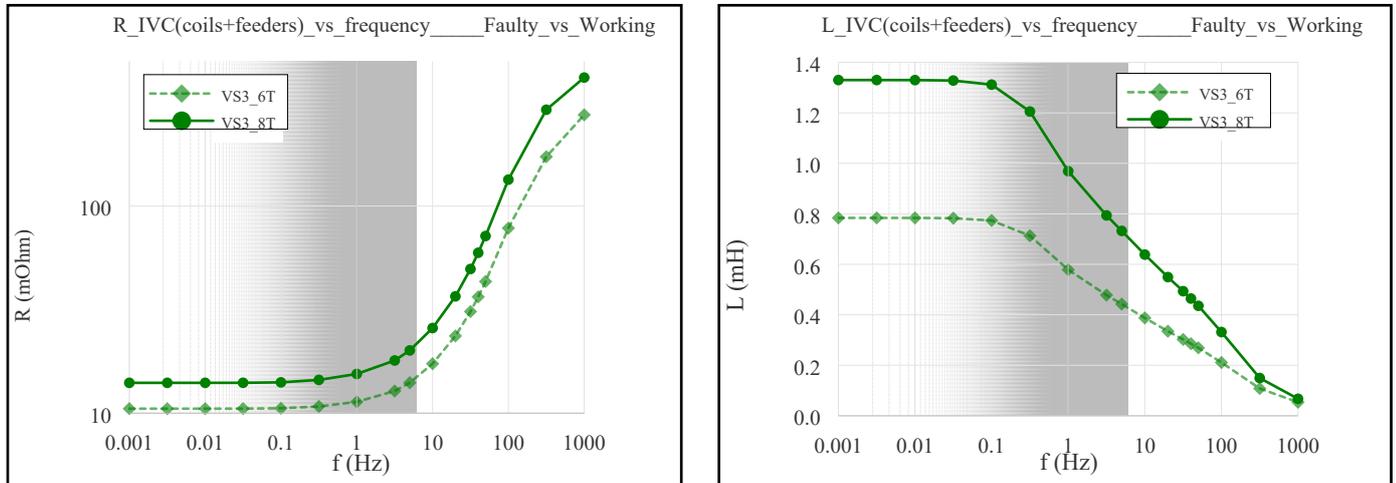**Figure 9-2: combined impedance of VS-coils and feeders for 8-turn and 6-turn configuration, including coupling with passive structures. Obtained from [RD45].**

9.2.4 Leakage resistance

The leakage resistance of the VS coils is strongly influenced by the nuclear radiation, with a reduction of the resistivity of the MgO insulation by 5 orders of magnitude: from 3.5E+06 down to 3.9E+01 MΩ*m. Further details are provided in [RD35].

In addition, the non-zero conductance of the Cooling Water Electrical Breaks also leads to leakage currents.

IO will provide final values in a more consolidated version of [RD46] in due course.

9.2.5 Grounding

All VS coil's steel cases are grounded to the Vacuum Vessel (VV) by their mounting bolts. The coil's cooling lines electrical breaks are also grounded on the side attached to PBS 26 through the PBS 26 cooling pipes.

9.3 Machine Assembly Tools (MAT, PBS 22)

The VS3 Power Supply will be installed in the area of Building 13 where the Sector Sub-Assembly Tools (SSATs) are currently located. The SSATs will be dismantled ahead of the VS3-PS installation phase. In order to preserve the possibility of reinstallation of these tools, PBS 41 and PBS 22 in charge of the Machine Assembly Tools, have made several arrangements in the corresponding Interface Sheet [AD78] in relation to the anchoring systems.

The VS3 Power Supply shall be designed taking into account all applicable requirements included in the Interface Sheet between PBS 22 and PBS 41 [AD78]. The design should take into consideration all relevant information in said document(s).

The following subsections highlight some of the main requirements and supplement the interface requirements in the interface documents.

9.3.1 Non-damaging of existing anchoring points

The installation of VS3-PS shall not result in any permanent damage to any of the existing anchoring systems type A, A1 and A2 described in section 10.1.3, which are designed for the fixation of the SSAT tools.

9.3.2 Visibility, marking and protection of existing anchoring points

In the Interface Sheet [AD78], PBS 22 is requested to provide and install protections on all remaining anchoring bolts and nuts type A, A1 and A2 for increasing visibility and for protection against shock (impact, collision). The installation of such protections should however not exclude the use of the respective anchors for the fixation of VS3-PS components. Protections shall be kept in place on all anchors not used by VS3-PS, whereas the protections/markings of the used anchors shall be stored for potential future restoring.

9.4 Component Cooling Water System (CCWS, PBS 26)

The VS3-PS shall interface with the PBS 26.CC cooling water loop CCWS-2A for component cooling purposes.

The VS3 Power Supply shall be designed taking into account all applicable requirements included in the Interface Sheet between PBS 41 and PBS 26.CC.2A [AD79]. The design should take into consideration all relevant information in said document(s).

The following subsections highlight some of the main requirements and supplement the interface requirements in the interface documents.

9.4.1 *Physical interfaces*

The location of the single physical interface point is provided in the 3D model [AD89]

The approximative coordinates of the interface point in TGCS are the following:

X-TGCS: -24048 mm

Y-TGCS: -63498 mm

Z-TGCS: -1047 mm
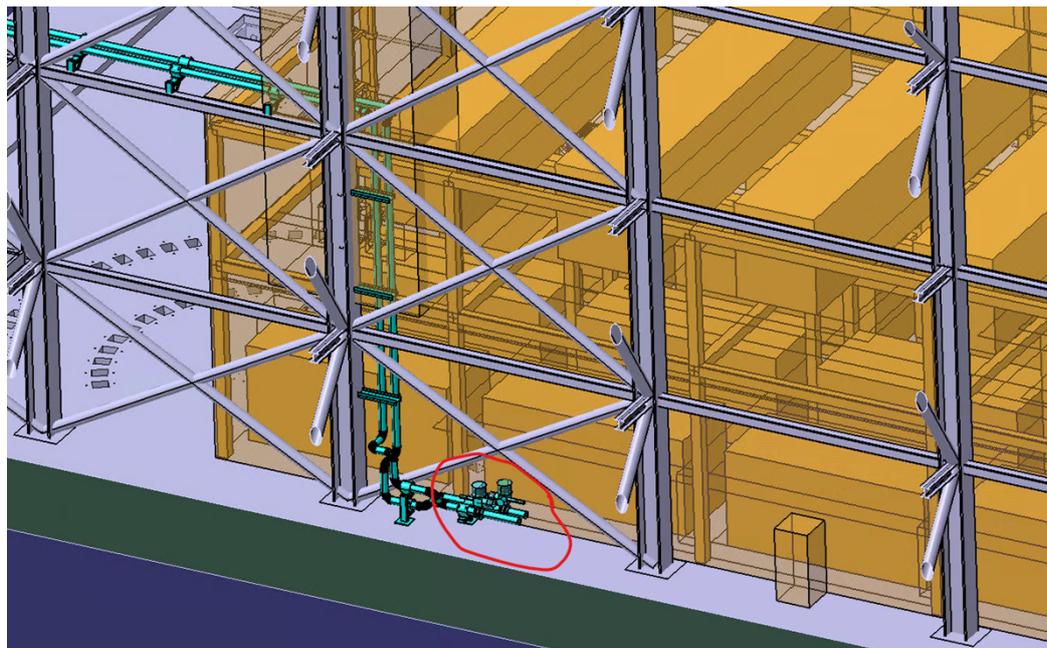
Figure 9-3: location of physical interface with PBS26 CCWS-2A (view from West to East of B13)

At the interface point, in accordance with 26CC2A-PID-001 [RD54], there are two isolation valves to which VS3-PS shall connect through welded connections on the counter flanges provided by IO:

- Isolation valve VC-1343 on PBS 26 inlet pipe
- Isolation valve VG-1344 on PBS 26 outlet pipe

For the connection to the PBS 26 cooling network, i.e. at the interface point, the same or equivalent (and compatible) materials shall be used. The characteristics of the pipes of PBS 26 cooling water network is provided in Table 9-4.

Table 9-4: physical characteristics of interface with PBS 26.CC

CCWS interface parameter	
Material type	Stainless Steel F316
Material – identification standard (norm)	ASTM A182
Material – provision standard (norm)	ASTM A182
Nominal diameter	DN 200

Thickness	Schedule 40s
Rating (nominal pressure)	ASME Class 150 [1]
Connection type	Flanged [2]
Note 1: equivalent to PN20 according to ISO-7005-1-1992 Note 2: IO provides the flange and the counter flange.	

The metallic parts in contact with the water provided by the Cooling Water System shall be copper or stainless steel. This requirement includes all VS3-PS internal components such as heatsinks, valves, etc). Inside VS3-PS cabinets and enclosures, the use of plastic pipes (or equivalent) is allowed.

Any isolation or bypass valve directly downstream the interface point shall be implemented with the same nominal diameter as the interface point (DN200).

Isolation valves shall be implemented upstream of each branch or VS3-PS subsystem in such a way that the subsystems or their internal components can be removed without interruption the flow and pressure inside the cooling water network.

The manifold(s) connected to each interface point shall be equipped with at least one spare isolation valve.

In case additional components such as isolation valves, specific connectors, etc. are used, the piping system shall be correctly designed according to the relevant standards to operate safely.

The DA shall weld their pipes to the interface point(s), in this case downstream the flange and counter flange, taking into account the welding requirements of section 14.

9.4.2   Mechanical supports and interface loads

The first support of VS3-PS cooling water pipes downstream the interface point shall be a fixed support in order to decouple the two interfacing cooling water systems. The first fixed support of VS3-PS shall be spaced in accordance with the calculated span under the provisions of section 8.8.3.

The connection between PBS 26 side and PBS 41 side may be through a rigid connection or through flexible hoses.

If a rigid connection is used, VS3-PS shall ensure that the mechanical loads at the last fixed support on PBS 26 side just upstream the interface point do not exceed the maximum allowable values (to be defined in a future version of [RD54], including the loads from the existing pipes on PBS 26 side). Piping stress analysis shall be performed up to this support by both systems, and the support will be designed taking into account the loads coming from both piping stress analyses.

The DA shall provide all necessary inputs and perform all necessary analysis to ensure that the interface loads remain acceptable for both interfacing systems.

9.4.3 Situation at the interface point

For the connection of the VS3-PS local cooling water network (DA scope) to the existing cooling water network CCWS-2A (IO scope), two options may be foreseen:

a. direct connection of the VS3-PS local cooling water network to IO's CCWS-2A network under the interface requirements described in this section and in [AD79]

b. connection through pressure control device(s), such as a Pressure Relief Device (PRD) or Pressure Limiting Device (PLD).

For the latter option, any such pressure control device would be under the full and sole responsibility of the DA, which includes but is not limited to the supply, the design (or selection of COTS), the installation, correct setting and commissioning, and the definition of the maintenance plan.

Should any discharge of water be necessary, the DA shall equally be responsible for the design, supply and installation of the drainage piping up to the interface point with IO's wastewater drainage system (refer to section 9.11.3), including all necessary mechanical protections and inline components to connect to IO's Industrial Drainage System in Building 13.

The space reservation for the installation of the DA drainage pipe will be provided by IO in the 3D model [AD89].

A possible concept for the interfacing of the local cooling water system of VS3-PS to IO's component cooling water system CCWS-2A is illustrated in Figure 9-4 below.
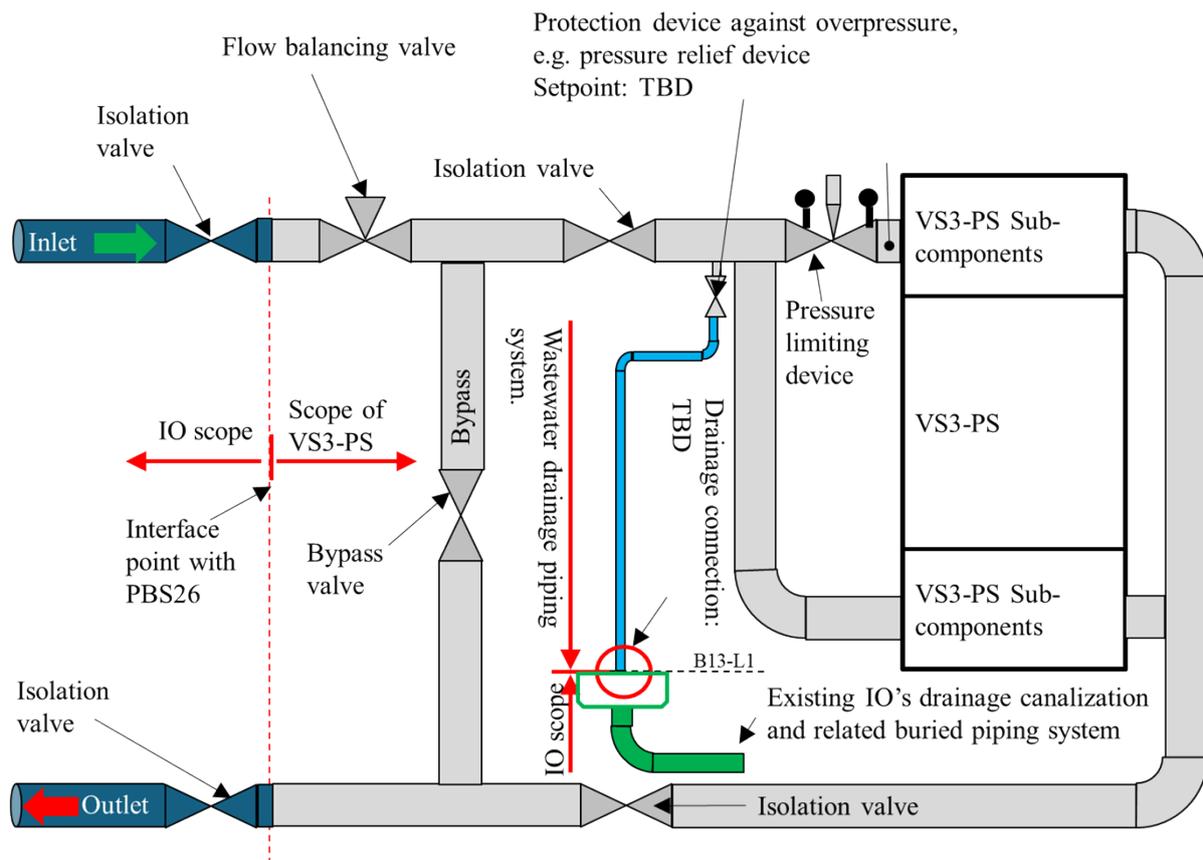

Figure 9-4: possible concept for the interfacing of PBS 26.CC.2A with the 41.V3 local cooling water system

9.4.4 Cooling water characteristics

The VS3-PS shall be designed to operate with the cooling water characteristics listed in Table 9-5.

Table 9-5: characteristics of the cooling water supply to VS3-PS

CCWS parameter	Value	Unit
Flow Rate (without dummy load)	21.6	kg/s
Flow Rate (with dummy load)	22.1	kg/s
CW Supply Pressure [1]	0.68	MPa(g)
Client System Design Pressure [2]	1.5	MPa(g)
Client System Pressure Drop (max. allowable at nom. flow)	0.4	MPa
CW Supply Temperature (max.)	31	°C
Return Temperature (max.)	33	°C
Note 1: the supply pressure refers to the steady-state pressure, which is the pressure after start-up of pumps or other transient events.		
Note 2: the maximum pressure at the interface point is not provided; the design pressure of 1.5MPa(g) already accounts for margin w.r.t. the aforementioned maximum pressure.		

9.4.4.1 Flow rate

The VS3-PS cooling water system shall be designed for the maximum flow rates of 22.1 kg/s and 21.6 kg/s for operation with and without dummy load, respectively.

9.4.4.2 Pressure

The expected nominal steady state pressure in the PBS 26 CCWS-2A cooling water network is 0.68 MPa(g). The transient pressure from PBS 26 supply can be as high as 1.25 MPa(g). The power supply shall not be damaged by this transient pressure.

The design pressure for all VS3-PS cooling water components directly downstream the interface with PBS 26 shall not be less than 1.5 MPa(g).

The VS3-PS cooling water system shall provide a means to regulate the flow through its components, for instance by implementing a flow balancing valve, so that the total flow is not perturbed and the pressure drop remains constant.

The test pressure for all components directly downstream the PBS 26 interface point, and not covered by additional protection devices, shall be no less than 2.25 MPa, which envelopes ANNEX I §7.4 of PED [CS31].

9.4.4.3 Temperature

The VS3-PS cooling water system shall be designed for a maximum supply temperature of 31 °C. The return temperature shall not exceed 33 °C.

9.4.4.4 Chemistry

The fluid conveyed in the CCWS-2A cooling water network is demineralized water, both for initial filling and as make up water. The conductivity of the cooling water at 25°C is <1 μS/cm.

9.5 ELM-PS MV Substation

The VS3 Power Supply receives the 22 kV input AC supply through the MV Substation that is part of the neighbouring ELM Power Supply (41.EL). This substation contains two MV cells dedicated to VS3-PS with configurable protections. VS3-PS has thus a physical and functional interface with ELM-PS MV substation for the connection and functional aspects such as measurements, control and protections. The functional aspects of the interface with the 22kV distribution network are provided in section 9.7 on the Pulsed Power Electrical Network.

9.5.1 Interface and boundary

The physical interface point is defined at the outgoing terminals of the MV cells; see Figure 9-5.
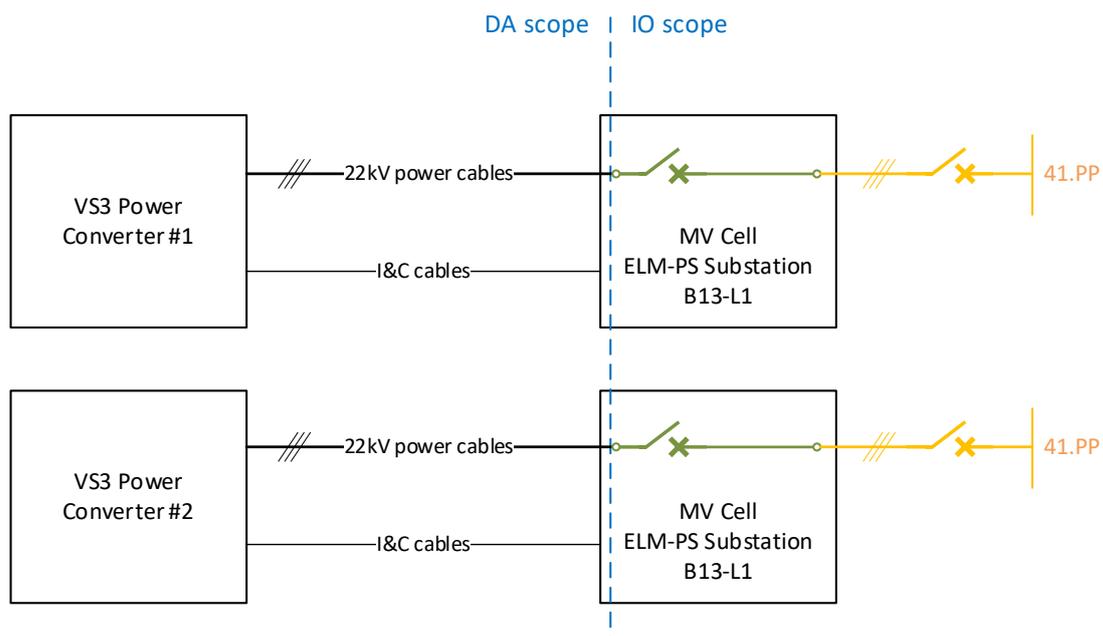
Figure 9-5: boundary between VS3-PS MV AC supply and MV cells of ELM-PS Substation at B1

The DA is responsible for the design, supply and installation of the MV power cable and I&C cables connecting the VS3 Power Supply to the MV cells of PBS 41.EL.MV, and for providing the parameter values of the protections in said MV cells, based on the necessary simulations. Additional details on the interface responsibilities are included in sections 5.2 and 9.9.

9.5.2 Conceptual description of MV Substation of ELM-PS (41.EL.MV)

The below subsections contain a preliminary description of the MV substation and the available facilities for VS3-PS. A dedicated interface document between VS3-PS and ELM-PS MV substation will be developed during the execution of the Task Agreement.

9.5.2.1 Substation and MV cells

Two MV cells are reserved in the ELM-PS MV Substation for MV supply to the VS3-PS, one for each power converter, see Figure 9-5.

Each of the two feeder cells of the VS3-PS system will allow the supply of an electrical load ranging between 0.5MVA and 3.5MVA, with the associated protections. The maximum power rating of each cell thus allows for significant margin with respect to the maximum input power of VS3-PS (specified in 6.1.2) maximum power supplied by PPEN (specified in section 9.7.2).
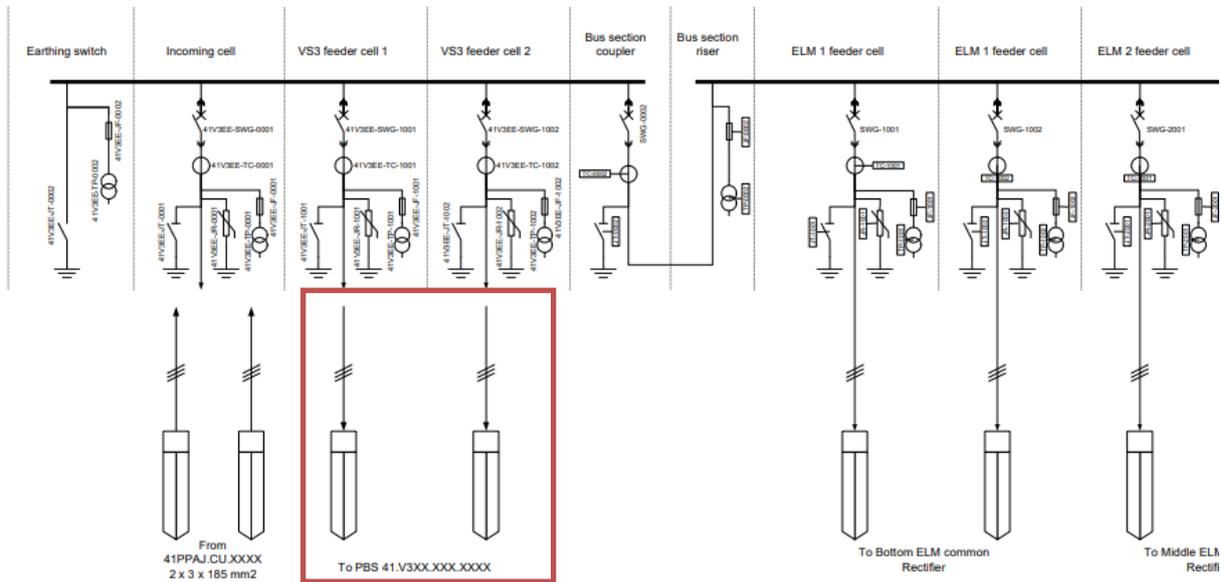
Figure 9-6: conceptual diagram of ELM-PS MV substation, with highlighted VS3-PS interface.

9.5.2.2 Circuit breakers and switches

Each circuit breaker and/or switch will be able to ensure the disconnection function as per NFC 13-200 [CS24], which imposes the minimum isolation distance between poles for ensuring the safety of operators.

9.5.2.3 Grounding switch

Grounding switches will be implemented on each distribution bus and in each MV cell.

9.5.2.4 Protection relays

The following protections will be available for implementation to protect the VS3-PS input stage:
   a. ANSI 49T or ANSI 49RMS: Overtemperature
   b. ANSI 87T: Differential protection

    c. ANSI 50: Short circuit protection
    d. ANSI 59N: Ground fault protection
    e. ANSI 67: Directional earth fault

The protections will be implemented using commercial protection relays that are directly interfaced with the MV circuit breakers.

Setting of the protection relays needs to be defined by the DA and subsequently transmitted to IO for integration within the ELM-PS MV Substation.

9.5.2.5 *Measurements*

The voltage of the distribution bus and the current in each branch upstream and downstream the distribution bus will be measured through sensors. VS3-PS may utilise these existing measurements. The type of interface – for instance a direct link between the plant control systems of ELM-PS and VS3-PS, or a link through ITER's Central I&C system – would then be defined in consultation with ELM-PS during the Task Agreement execution.

9.5.2.6 *Interlocks*

A Mechanical Key Interlock System (MKIS) will be implemented to avoid dangerous configurations for the MV distribution system as well as for workers and operators. One of these configurations is the interconnection of the two 22kV PPEN feeders in parallel through the two distribution buses and the bus coupler.

The MKIS will be able to lock the earthed position of the feeder cells independently for each downstream system, including VS3-PS.

The first key of the MKIS which allows starting the energization sequence of the VS3-PS system will be a free key, brought from the MV substation to the central IO control room to coordinate the energization of systems.

The MKIS will be integrated in the existing MKIS implemented at IO. The existing system is based on the RONIS product line, provided by Secum Interlock. A similar, or equivalent (and compatible), system will be used.

9.6 VS3 Extension and IVC Busbars (PBS 41.V3.BE, 41.V3.BB)

The VS3 Extension Busbars connect the VS3-PS in Building 13 to the VS3 Linkboard at Building 11-L4. From the Linkboard, the connection to the VS coil turns is made through the IVC Busbars. The IVC Busbars are designed in accordance with the Technical Specification of [RD59]; the VS3 Extension Busbars in accordance with [RD60].

The interface physical details (location, terminal hole patterns, etc.) and functional requirements (e.g. overtemperature protection) are provided in the Interface Sheet between VS3 Power Supply (41.V3) and VS3 Busbars (41.V3.BB / 41.V3.BE) [AD81]. The VS3 Power Supply shall be designed taking into account all applicable requirements included in that document.

The following subsections highlight some of the main requirements and supplement the interface requirements in the interface documents.

9.6.1 *VS3 Extension Busbars – Physical Interface*

The interface point between the VS3 Extension Busbars (41.V3.BE) and VS3 Power Supply (41.V3) is at the terminals of the busbars. The physical interface point is located slightly above the VS3-PS space reservation, to aid the independent installation of both systems. Further details and the latest coordinates are contained in the CMM [AD89].

9.6.1.1 *Global situation and layout*

Figure 9-7 illustrates the global situation, Figure 9-8 shows the approximate location and preliminary implementation of the interface point.
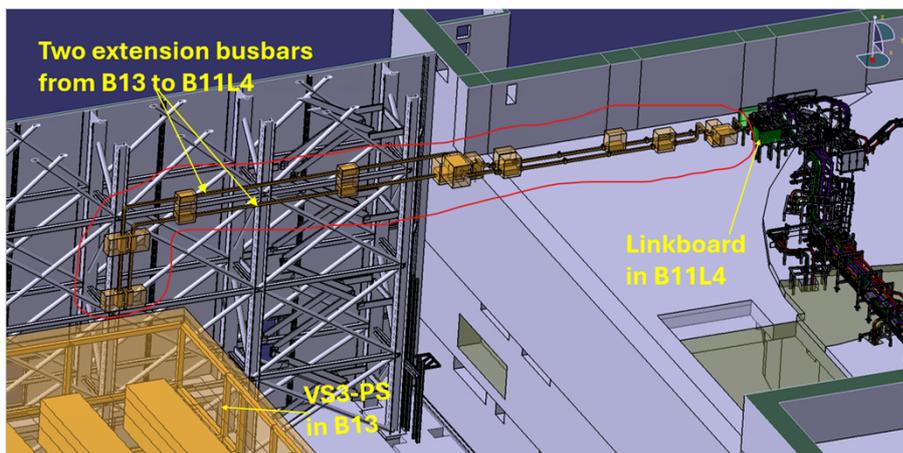

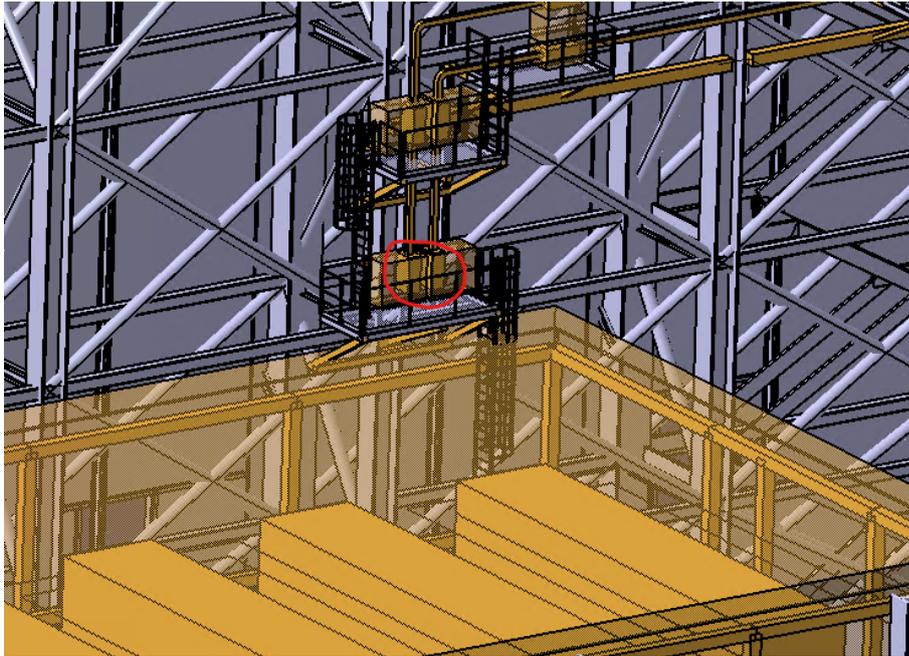**Figure 9-7: overview of VS3 Extension Busbars between B11-L4 and B13**

Figure 9-8: interface point between VS3-PS and VS3 Extension Busbars (enclosures at highlighted location to be provided under this Task Agreement)

9.6.1.2 Physical interface and connection

At the interface point, the VS3 Extension Busbars provide two solid copper terminals per busbar to which the conductors of VS3-PS (e.g. cables, busbars) shall be connected by the DA.

The VS3 Extension Busbars also provide a flange immediately upstream of the terminal breakout to allow for the installation of an enclosure as per section 9.6.1.5.

9.6.1.3 Flexible connection

The VS3-PS conductors connecting to the Extension Busbar terminals shall be connected through a flexible connection solution to mechanically decouple both systems and thereby limit the transfer of additional mechanical loads to the terminals.

The flexible connection shall be capable of accommodating all thermal expansion and contraction, as well as all relative displacements between the first support on VS3-PS side (mechanical fixed to the VS3-PS Main Steel Structure) and the last support of the Extension Busbar (mechanically fixed to Building 13).

9.6.1.4 Interface loads

The DA shall provide the mass participation of the VS3-PS components between the last support of the Extension Busbars and the first support at the VS3-PS side for integration in the IS [RD60] and consequently the design of both interfacing system.

9.6.1.5 Enclosure

At each Extension Busbar end, the DA shall design, supply and install an enclosure that encloses all exposed conductive parts. The enclosures shall be attached to the flanges at the busbar ends and shall feature removable panels for inspection and maintenance purposes.

The design of the enclosure shall, together with the selected conductor solution, ensure that the surface temperature of the enclosure does not exceed the limits imposed by NF C 15-100 [CS25].

PBS41.V3.BE will provide the flanges and the terminal at the end of the Extension Busbars, and will provide the associated definition drawings.

9.6.2   VS3 Extension & IVC Busbars – Functional Interface

9.6.2.1   Rated Voltage and Test Voltage

The Extension Busbars and IVC Busbars are designed for a rated system voltage of 2700V, between poles and pole to case, and tested to 6.4 kV (ACrms) for 1 minute.

The VS3-PS shall be designed so to ensure that the rated system voltage of 2700V is not exceeded at any time during operation. This requirement is enveloped by the voltage ratings of the VS coil system.

9.6.2.2   Rated Currents and Fault Current

The Extension Busbars and IVC Busbars are designed for a rated RMS current (continuous duty) of 15 kArms, a pulsed operating current waveform with a peak of 83 kA and a maximum fault current of 120 kA for 100ms.

The VS3-PS shall be designed so to ensure that the aforementioned rated and fault current levels are not exceeded at any time during operation. This requirement is enveloped by the admissible current levels of the VS coil system.

9.6.2.3   Overtemperature protection

The VS3 Power Supply shall prevent overheating of both the Extension Busbars and the IVC Busbars through the implementation of the relevant protection functions. This protection is covered in section 6.4.3.7 (Busbar Overtemperature Protection).

The required I&C interfaces for the cooling water flow switches and temperature sensors are specified in the following section.

9.6.3   I&C interfaces and requirements

Flow switches and temperature sensors are integrated into each Cooling Water Collector (CWC) to which the integrated cooling water channels of the busbar segments are connected. Details on the location, type and number of sensors are included in the Interface Sheet between VS3 Power Supply (41.V3) and VS3 Busbars (41.V3.BB / 41.V3.BE) [AD81].

9.6.3.1   Number and type of sensors

The VS3-PS shall be interfaced with all flow switches and temperature sensors associated to the VS3 Extension Busbars and the VS3 related IVC Busbars, as documented in [AD81]. A summary of the current version is included in Table 9-6, for information.

Table 9-6: number and type of IVC and Extension Busbar sensors to be interfaced by VS3-PS [AD81]

Type	Busbar	Count	Sensor reference
Flow switches	Extension Busbars	4	Eletta V1-FS25-65C/RL-E
	IVC Busbars	40	
Temperature sensors	Extension Busbars	4	3-wire RTD (Pt100), SEN-111C
	IVC Busbars	40	

9.6.3.2 *Routing from B11-L4 to the interface point at B13*

The signal cables of the flow switches and temperature sensors are terminated in Signal Terminal Boxes located at B11-L4.

The routing of all IVC and Extension Busbar flow switches and temperature sensors signal wires from B11-L4 to the interface point in the VS3-PS area in Building 13 is in the scope of IO, and included in the Interface sheet between VS3 Power Supply (PBS 41.V3) and Cable Tray System (PBS 44) [RD36] and the associated cable diagram(s).

The cables between B11-L4 and B13 are I&C-type cables, referenced in the IO Cable Catalogue under T3xx16LR with xx being the number of wires per cable, with overall shield and individually shielded twisted triads with wire cross-section of 1.5mm2. As per [RD36], the number of triads per cable depends on the number of sensors associated to the Signal Terminal Boxes.

9.6.3.3 *I&C interface point*

The I&C cables are terminated in a cubicle tagged "41V3IC-CU-4001", to be supplied by the DA, inside the VS3-PS space reservation, see Figure 9-9.

The DA shall supply and install the I&C cubicle and the necessary wire terminals for termination of the cables originating from B11-L4. IO (PBS 44) is responsible for installing these cables into the supplied terminals.

The I&C cubicle 41V3IC-CU-4001 is reserved for the termination of the Busbar I&C and the required I&C hardware for data acquisition. Other I&C equipment may be installed inside this cubicle under the condition that the signal integrity and reliability of the Busbar I&C is not affected.
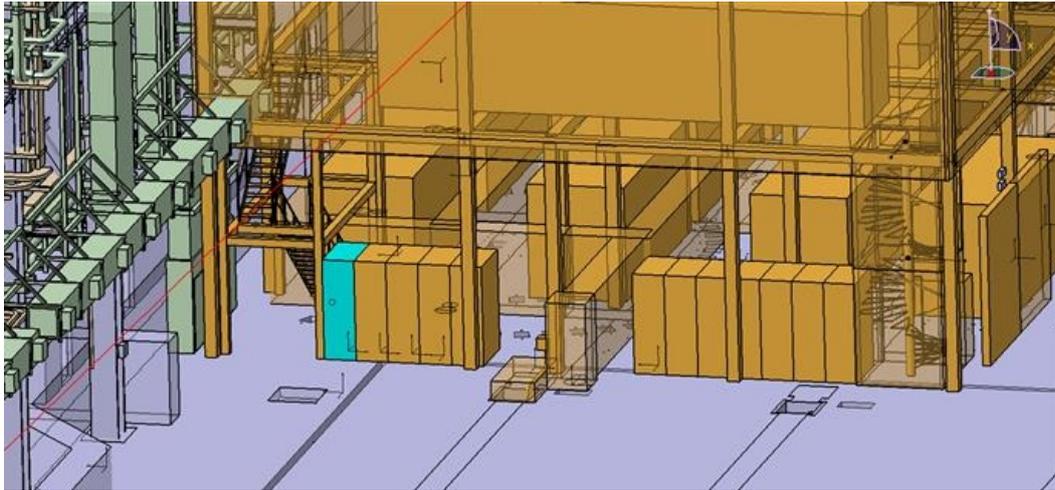
Figure 9-9: reserved cubicle 41V3IC-CU-4001 for termination of Busbar I&C cabling

9.6.3.4 Data acquisition

The VS3-PS PIS shall acquire all sensor data at the appropriate rate and with sufficient accuracy and precision to implement the overtemperature protection function.

The abnormal status of a busbar segment shall be reported.

Temperature sensor signals shall be individually acquired and made available in the VS3-PS I&C system.

9.7 Pulsed Power Electrical Network (PPEN, PBS 41.PP)

The PPEN transforms and distributes power from the incoming 400 kV 50Hz AC supply grid to the 66kV and 22kV levels of the pulsed power loads of ITER.

The VS3 Power Supply shall be designed taking into account all applicable requirements included in the Interface Sheet between PBS 41 IVC Power Supplies and PBS 41.PP [AD80]. The design should take into consideration all relevant information in said document.

The following subsections highlight some of the main requirements and supplement the interface requirements in the interface documents.

9.7.1 General characteristics and power quality

The VS3 Power Supply shall be designed to operate with the characteristics and operational ranges of the MV AC supply listed in Table 9-7.

Table 9-7: general characteristics and power quality of 22 kV AC supply

Parameter	Value
AC Supply voltage	22 kV ± 10 %
Grid frequency [1]	50 Hz ± 1 %
Short-circuit current [2]	28 kArms
Total Voltage Harmonic Distortion (THDv)	< 8%
Grounding system	IT

Note 1: larger frequency variations up to -6%/+10% are possible, yet operation outside of stated range is not required [41s282-R, [AD4]]

Note 2: at interface point between PPEN feeders (41.PP) and input terminals of MV Substation (41.EL.MV)

9.7.2 Maximum power

The VS3 Power Supply shall be designed and operated to respect the maximum apparent power available through the 22 kV AC connection as defined in Table 9-8. The distribution of power between the two power converters comprising the power supply is not constrained.

Table 9-8: maximum apparent power available to VS3-PS

PPEN 22 kV	Maximum apparent power Sn
VS3 Power Converter #1	3.7 MVA (combined)
VS3 Power Converter #2	

9.7.3 Inrush current

The inrush current during the energization of VS3-PS shall not exceed ten times the rated current, the latter being defined as the rms current level at the nominal apparent operating power and at the nominal supply voltage.

9.7.4 Harmonic distortion

The Total Harmonic Distortion on the supply current (THDi) caused by VS3-PS operation shall not exceed 6%, with THDi defined as the ratio of the square root of the sum of all harmonic current components squared and the fundamental current component.

Harmonics distortion rates are to be measured in accordance with IEC 61000-4-30 and IEC 61000-3-6 with a time interval of 10 minutes.

9.7.5 I&C

The VS3 Power Supply shall be interfaced with the upstream switchgear in the ELM-PS MV Substation through hardwired connections, for permissive/status signals and circuit breaker (trip) commands.

9.8 Steady-State Electrical Network (SSEN, PBS 43)

The auxiliary power of all VS3 Power Supply components is provided by the Steady-State Electrical Network. The VS3-PS interfaces with SSEN for both Class IV as interruptible supply for Ordinary Loads and for Class II-IP as uninterruptible supply for Investment Protection Loads.

The physical interface between VS3-PS and SSEN is defined at the end of the PBS 43 feeder cable. More precisely, the boundary is at the point where the PBS 43 supplied, installed and terminated power cable is connected to the main circuit breaker of the LV distribution cabinets of VS3-PS, refer to Figure 9-10.
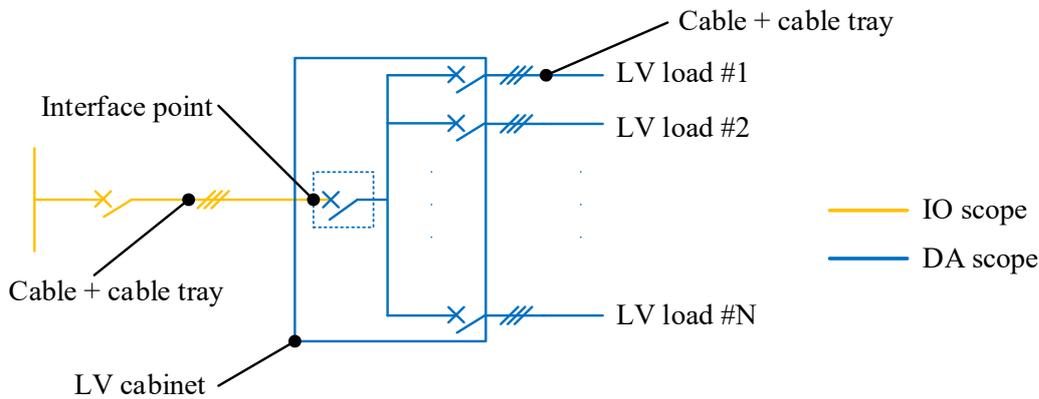
Figure 9-10: definition of the physical interface point between VS3-PS and SSEN (PBS 43)

Note on Figure 9-10: in accordance with NF C 15-100 [CS25], the neutral shall be switched together with the phase conductors.

The supply of Class IV and Class II-IP power to the auxiliary power loads of VS3-PS is accomplished through two SSEN feeders, one for each supply type, as per Table 9-9.

Table 9-9: interface points with SSEN and allocated power

Location	Distribution Board	Nominal Input Power	Power Factor	Supply Type	Rated Nominal Voltage	IS
B13-L1	DB-Class IV for VS3-PS	35 kW	0.85	Class IV – Normal Ordinary Loads	400 VAC / 50 Hz / 3 phase	IS-43-41-501 [AD82]
B13-L1	DB-Class II for VS3-PS	10 kW	0.85	Class II – UPS & Batteries Investment Protection Loads	400 VAC / 50 Hz / 3 phase	IS-43-41-502 [AD83]

The planned location of the physical interface points is at the most southern position inside the VS3-PS space reservation in Building 13, where most of the cubicles are anticipated, see Figure 9-11. The final and exact location are to be defined during the detailed design stage.
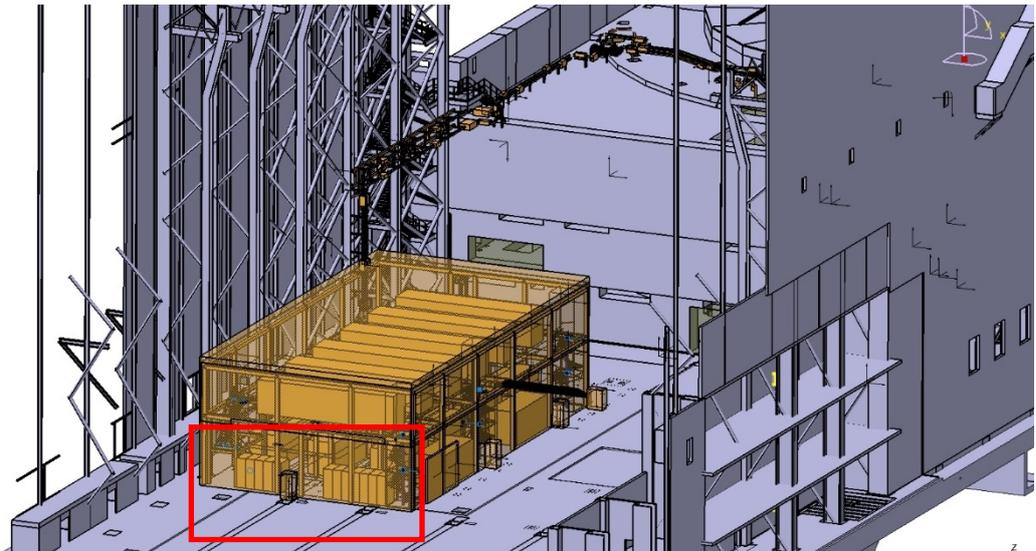
Figure 9-11: anticipated location for LV distribution and I&C cubicles

The DA is responsible for the LV distribution to all SSC's within their scope requiring LV auxiliary power. The design of the LV distribution system shall comply with all applicable codes and standards, most notably NF C 15-100 [CS25], EDH Guide A [AD17] and EDH Guide C [AD18].

The DA is responsible for ensuring the short-circuit current withstanding, the coordination between upstream/downstream protections, the respecting of cable bending radii, the termination type and sizing of the supplied components, with adequately considering the integration with the upstream SSEN system.

Details on the LV design (client list, power cables, circuit breakers, etc.) shall be provided at each design gate for review by PBS 43. Prior to the connection to IO's SSEN system, protection coordination analysis shall be performed and submitted using the CANECO BT software.

The VS3 Power Supply shall be designed taking into account all applicable requirements included in the Interface Sheets between PBS 41.V3 and PBS 43 Class II-IP [AD83] and Class IV [AD82]. The design should take into consideration all relevant information in said documents.

The following subsections highlight some of the main requirements and supplement the interface requirements in the interface documents.

9.8.1   General characteristics and power quality

The VS3-PS components requiring LV auxiliary power and the LV distribution system shall be designed or selected to operate with the nominal ratings, variations and power quality defined Table 9-10.

Table 9-10: general characteristics and power quality of SSEN LV supply

Parameter	Value
AC Supply voltage	400 V ± 10 %
Grid frequency [1]	50 Hz ± 1 %
Short-circuit current	< 36 kA
Total Voltage Harmonic Distortion (THDv) [2]	< 5%
Grounding system	TN-S
Incoming cable configuration	3 Ph + N + PE

Note 1: larger frequency variations are (exceptionally) possible

Note 2: harmonics distortion measured in accordance with IEC 61000-4-30 and IEC 61000-3-6 with a time interval of 10 minutes.

9.8.2 Auxiliary power consumption

The auxiliary power required by VS3-PS for Ordinary Loads and Investment Protection Loads shall not exceed the power levels allocated with PBS 43 – SSEN, listed in Table 9-9.

The power factor at each interface point with SSEN shall not be less than the values listed in Table 9-9.

9.9 Cable Tray System (CTS, PBS 44)

9.9.1 Cables and Cable Trays

The VS3-PS system is interfaced with IO's Cable Tray System for the following two purposes:

9.9.1.1 I&C cables between VS3 Busbars and VS3-PS

The cables between the Signal Terminal Boxes of the VS3 IVC and Extension Busbar at B11-L4 and the interfacing cubicle in the VS3-PS space reservation at B13, as per IS-41.V3-44-001 [RD36]. The supply and installation of these cables are under IO responsibility.

9.9.1.2 MV feeders and hardwired I&C cables for switchgear

The MV cables and switchgear-related I&C cables between the ELM-PS MV Substation and the AC input side of VS3-PS are in the scope of this Task Agreement, for which the DA shall liaise and agree with PBS 44 and define all necessary interface requirements for a dedicated interface sheet that will be part of the existing ICD-41-44 [RD66]. IO will develop the IS based on the interface requirements defined by DA.

The responsibilities are defined as follows:

     o Main cable trays between VS3-PS and ELM-PS in B13: IO (PBS 44)

     o Local cable trays from main cable trays up to:

- - - the boundary of VS3-PS: IO (PBS 44)
    - the boundary of ELM-PS: IO (PBS 44)
  - Internal cable trays from:
    - boundary of VS3-PS to MV equipment endpoint: DA
    - boundary of ELM-PS to MV substation: IO
  - Design and supply of MV and I&C cables: DA
  - Installation of MV & I&C cables: DA

The internal cable trays used to support cables inside the space reservation of the VS3-PS system, and which do not belong to the two categories described hereabove, are in the scope of this Task Agreement and do not need to be interfaced with PBS 44.

9.9.2   PBS 44 Cable Trays to be supported by Main Steel Structure

The PBS 44 Cable Trays supporting the MV, LV and I&C cables that are routed from east to west in Building 13 shall be supported by the VS3-PS Main Steel Structure (MSS) as conceptually shown in Figure 9-12.
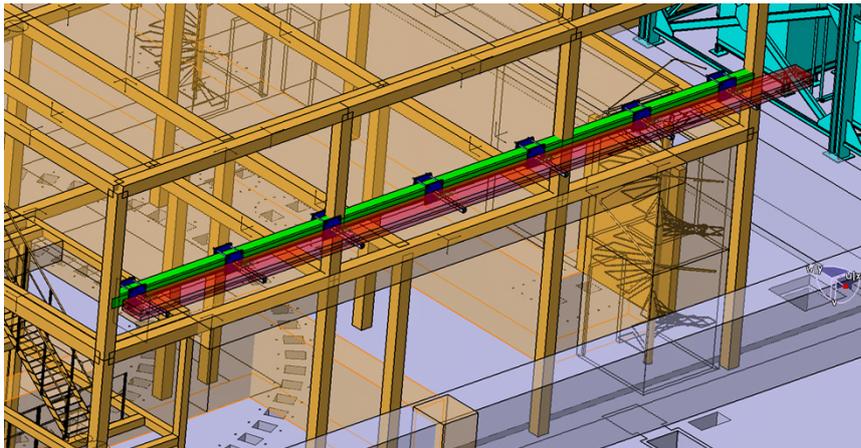

Figure 9-12: conceptual drawing of PBS 44 cable trays supported by VS3-PS Main Steel Structure

9.9.2.1   Horizontal beam to be provided by VS3-PS MSS

The VS3-PS MSS shall provide a horizontal primary or secondary steel structural member to which PBS 44 can attach the clamps for the support of the cable trays.

The vertical position of this support beam shall range from 5.0 to 7.0 meter and shall allow the cable tray system to cross the cask trajectory (east side of VS3-PS) at a height of approximately 6.0 meter.

The MSS and horizontal beam shall be designed such that it does not preclude the support of the additional loads associated with a bridge structure spanning the 8m wide cask trajectory, attached to the VS3-PS MSS on one side and an adjacent steel structure on the other side.

Figure 9-12 shows the horizontal beam as dedicated (secondary) steel member; however, a primary steel member positioned at the appropriate height and offering sufficient accessibility may also be considered.

9.9.2.2 Characteristics of the cable trays and associated support system

The linear dead load of the cable trays is approximately 200kg/m.

The cantilever beams have a maximum length of 1.0 meter.

The spacing between consecutive cantilever beams is approximately 2 meter.

The attachment of the cantilever beams to the horizontal beam may be based on bolted dual-plate clamping arrangements (see Figure 9-13) or welded plates.
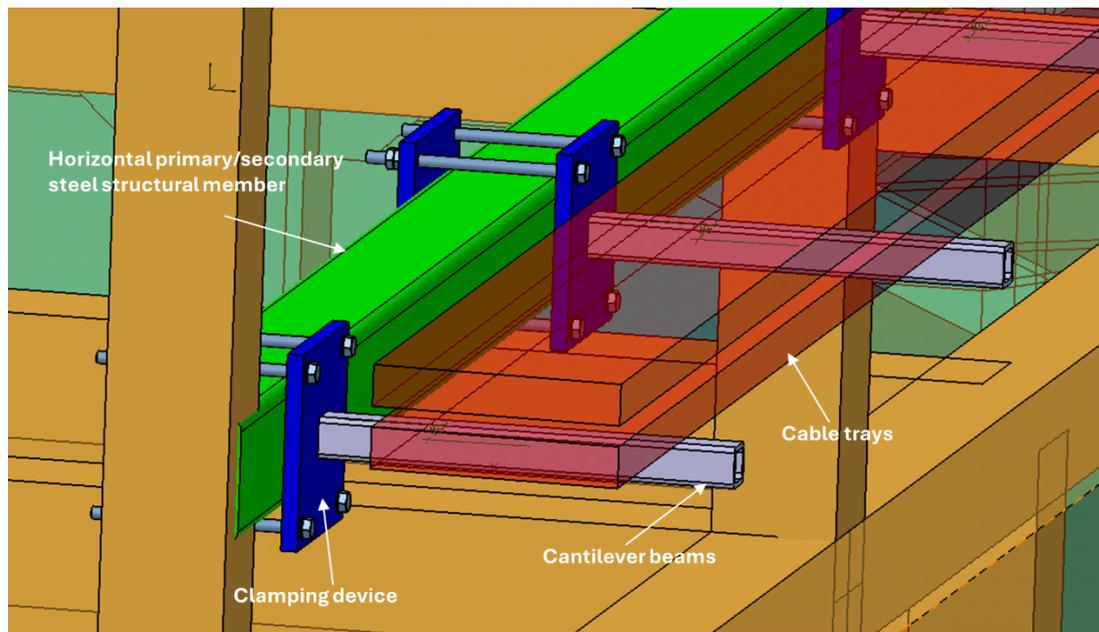

Figure 9-13: conceptual drawing of cable tray support components

9.9.2.3 Schedule and installation sequence

The cable trays may only be installed once the MSS has been erected; however, certain adjacent systems may require energization earlier, necessitating the availability of their cables in advance. In such cases, the cables may be temporarily placed on the floor pending their final installation in the cable trays. This may affect the installation activities associated with VS3-PS and shall therefore be considered in the installation sequence and schedule.

9.9.2.4 Responsibilities

The clamps, cable tray support beams and cable trays are provided and installed by PBS 44.

The responsibilities for VS3-PS are limited to providing the horizontal primary/secondary steel structural member capable of supporting the cable tray system along the width of the VS3-PS space reservation, and ensuring the cable trays and clamping system can be installed with the specified spacing once the MSS has been erected.

The details are to be agreed between the DA and PBS 44 during the detailed design phase.

9.10 Interface with Central I&C System

The ITER I&C System refers to all hardware and software required to operate the ITER machine, comprises the VS3-PS I&C systems (namely Plant System I&C in applicable documents), the Central I&C systems and the I&C networks, as depicted in Figure 9-14.
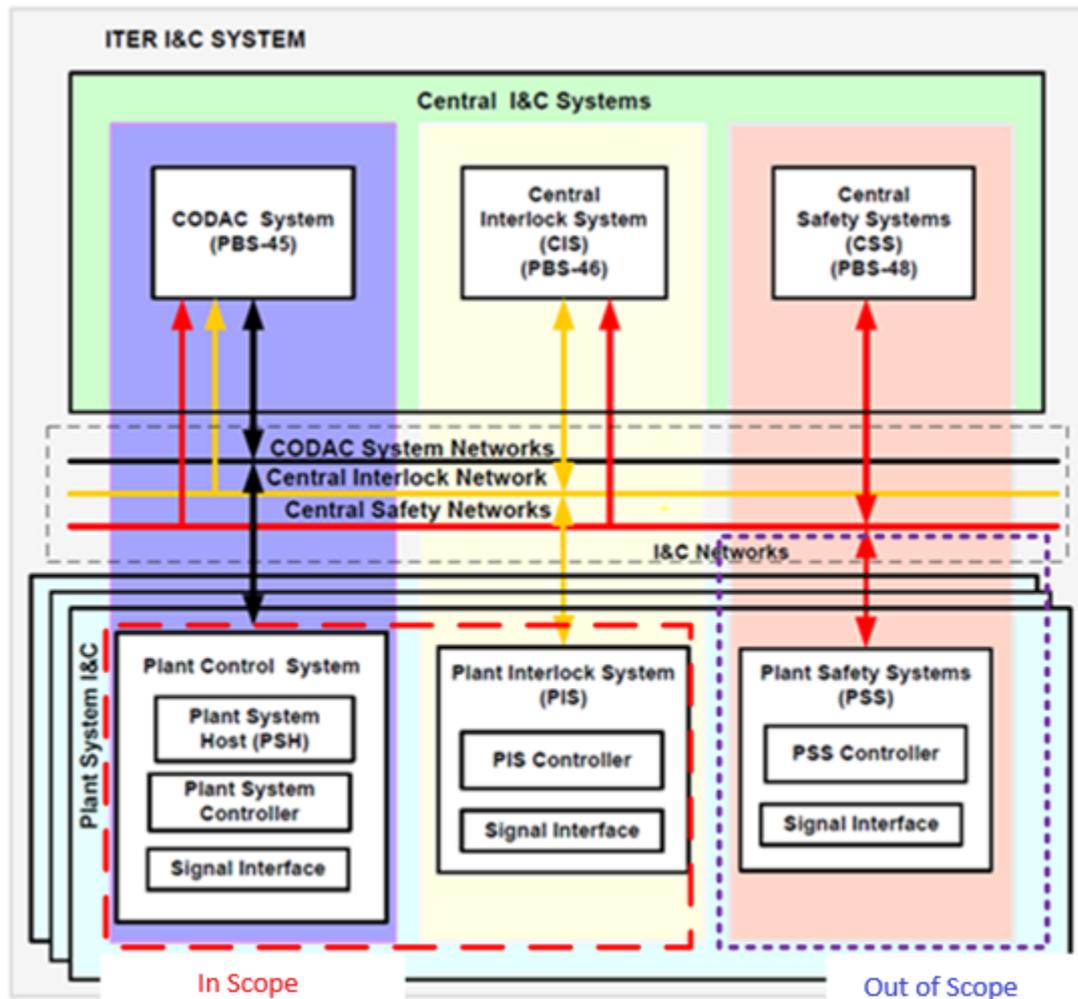
Figure 9-14: ITER I&C Systems - CODAC System, Central Interlock System, Central Safety Systems and plant systems I&C. Adopted from 18[AD46].

The main systems involved in the ITER I&C System are:

1. Central Interlock System (CIS): provides plant-wide investment protection functions. It communicates with the Plant Interlock Systems, using the Central Interlock Network and provides status to CODAC System. The CIS provides all HMIs for the visualization of the status, and override of Interlocks. The release (of latched interlocks) is controlled via CODAC. Interface information and related requirements are defined in section 9.10.2.

2. Central Safety System (CSS) provides plant-wide nuclear and occupational safety functions and usually communicates with Plant Safety Systems using Central Safety Network. Instead of a MKS (Mechanical Key System) a signal might be foreseen – this should be requested through the HIRA.

3. COntrol, Data Access and Communication (CODAC) system is the central (supervisory) control system for the conventional plant control systems of the ITER I&C architecture. Conventional control refers to all hardware and software that do not relate to Central Interlock System and Central Safety System. Interface information and related requirements are defined in section 9.10.1.

The interface points with the ITER central I&C systems are in the VS3-PS plant I&C cabinets, as shown in Figure 9-15.
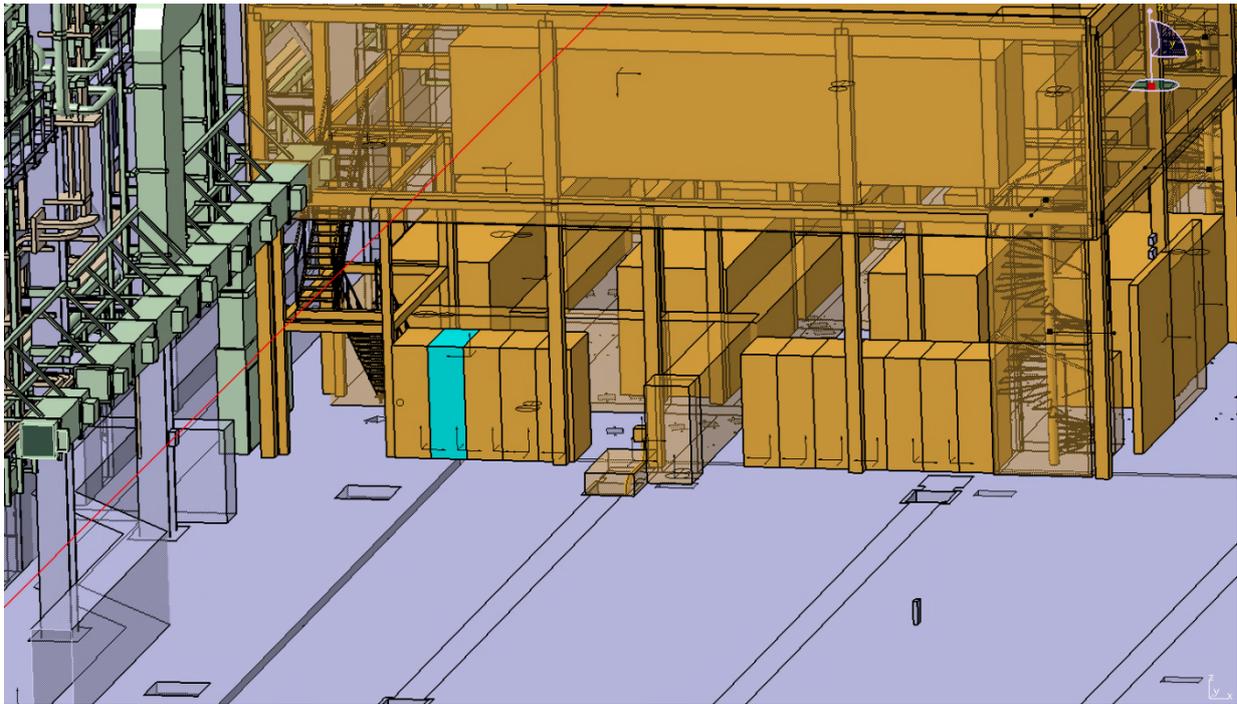
Figure 9-15: anticipated location of the interface points with CODAC and CIS (highlighted cubicle), as per [AD84]

The foreseen number of interfaces points is defined in section 6.1 and 6.2 of [AD84].

9.10.1 Control, Data Access and Communication (CODAC, PBS 45)

The CODAC system provides plant-wide data monitoring, alarm handling, error logging, data visualization, data handling, data storage, global operation state management, operation schedule management, automated pulse execution and plasma control functions for the overall operation of the ITER machine with all its subsystems (including the VS3-PS system).

All these functions for the complete ITER machine are operated via Human Machine Interfaces on CODAC Terminals. All CODAC terminals are located in the Main Control Room of ITER, except during the construction and commissioning phases, during which limited access to CODAC terminals will be provided to the DA in Building 13.

CODAC also provides the technical platform for the Plasma Control System.

CODAC provides the physical and logical interconnection for the VS3-PS Plant Instrumentation and Control System (see details of VS3-PS Instrumentation and Control systems in section 7.9) with the CODAC Networks consisting of:

1. PON – Plant Operations Network: all signal states, commands, data to be available or to be visualized, error, alarm and system states are transmitted here. The protocol used is EPICS. The local PLCs / controllers are interfaced with OPC UA.
2. DAN – Data Acquisition Network: high bandwidth data archiving network for scientific or technical purposes.

TCN and SDN are the PCS network interfaces (see section 9.10.3), where SDN is used for high-frequency, low-latency, low-jitter communication, and TCN for time synchronization by providing a high precision time reference.

All data on PON, SDN and DAN is archived. Tools for immediate or historic examination and visualization are provided by CODAC.

The VS3-PS plant shall be interfaced with CODAC to:

1. Receive state transition commands,
2. Receive setpoints and send status and TCN timestamped voltage/ current readings via SDN,
3. Send the status of the plant including alarms and errors,
4. Log data for tuning or calibration,
5. Ensure that the system can be operated in an integrated way with CODAC,
6. Provide the data for the commissioning and plant control HMIs for VS3-PS,
7. For receiving configuration parameters via PON (and CIN for interlock systems).

The VS3 Power Supply shall be designed taking into account all applicable requirements included in the Interface Sheets between PBS 41.V3 and PBS 45 [AD84][AD80]. The design should take into consideration all relevant information in said documents.

The DA shall be accountable of developing the interfaces between the VS3-PS system and CODAC. The scope of supply for the interface between the VS3-PS system and CODAC is shown in Figure 9-16. In general, the DA is responsible for the supply of the I&C cabinets, rack, switches or controllers, whereas the IO is responsible of pulling the optic fiber till the connection point.
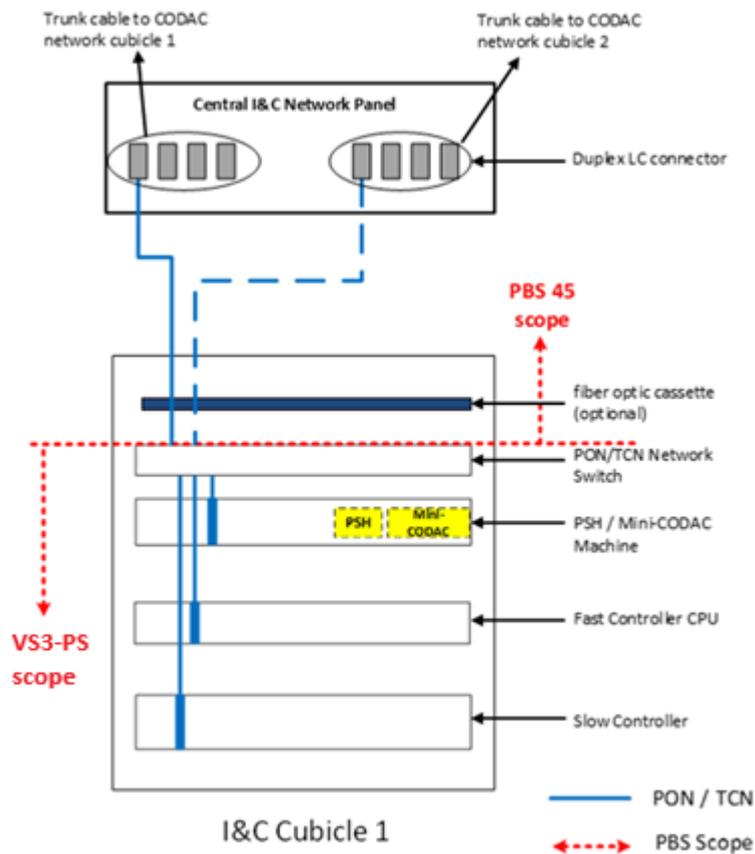
Figure 9-16: scope of supply for the interface between the VS3-PS system and CODAC

9.10.2 Central Interlock System (CIS, PBS 46)

The ITER's Central Interlock System (CIS) provides plant-wide investment protection functions, communicates with Plant Interlock Systems using Central Interlock Network (CIN).

The VS3-PS Plant Interlock System shall be interfaced with CIS to:

a) Receive the interlock events from CIS
b) Coordinate the received events and transmit the interlock actions
c) Inform the operation about the status of all interlock functions
d) Log all critical data
e) Ensure ITER interlocks can be operated in an integrated way with the VS3-PS PIS through a central HMI capable of performing operator actions like: permits, resets, overrides, etc.

The physical interfaces of VS3-PS with CIS shall be as follows:

- Network architecture (packet switched) interface between VS3-PS PIS (PLC's and Fast-Host servers) and CIS
- Point-to-Point fibre optic links for the fast architecture (cRIO to cRIO), between VS3-PS fast-PIS and CIS

The DA shall develop the interfaces between VS3-PS and the CIS as per the applicable procedures [AD48], which explicitly includes performing all necessary risk assessments and the definition and declaration of interlock actions and events using the relevant document templates.

The VS3 Power Supply shall be designed taking into account all applicable interface requirements included in the Interface Sheet between PBS 41 and PBS 46 [AD85]. The design should take into consideration all relevant information in said document.

As per Table 9-1:
- IO is responsible for the maintaining of IS-41-46-009 – Interface Sheet (IS) between V3PS Plant Interlock System of PBS41 and PBS46 [AD85] based on the relevant data that shall be provided by DA;
- DA is responsible for the creation and maintaining of the Interface Data Sheet IDS-41-46-009 associated to [AD85], and all interlock event/action documentation

9.10.3 Plasma Control System (PCS, PBS 47)

The VS3 Power Supply is interfaced with the Plasma Control System (PCS) for the operational control of the system during plasma pulse operations. The physical interface is established through the CODAC networks, including TCN for timing and SDN for deterministic and high data rate communication, which provide the technical platform for the PCS.

The interface between VS3-PS and PCS is managed through the following interface management documents:
- IS-47-41-005 [AD86] for functional and architectural requirements
- IS-47-41-006 [AD87] for a detailed description of the information/signals including signal functions and characteristics

In accordance with Table 9-1, IS-47-41-006 shall be developed by the DA as part of the design process and subsequently maintained through to the final commissioning stage.

The interface requirements in IS-47-41-005 are generally incorporated into this technical specification; however, the DA remains fully responsible for ensuring full compliance with all interface requirements contained in that document.

The following subsections highlight some of the main and specific requirements, and supplement the interface requirements in the interface documents.

9.10.3.1 VS3-PS behaviour when not required to operate

The VS3 Power Supply shall prevent any current from circulating in the VS3 coil circuit when the system is not required to operate during a Tokamak pulse. This requirement applies to all coil turns actively connected to the power supply through the VS3 Linkboard, and for (induced) coil circuit voltages not exceeding the nominal DC Link voltage.

9.10.3.2 Measurements

The VS3 Power Supply shall provide all voltage and current signals that are essential to plasma control, with the sensors and technical characteristics as propagated in section 7.9.1.

9.10.3.3 Status monitoring and reporting

The VS3 Power Supply shall report to PCS its operational status with an update rate of at least 100 Hz.

9.10.3.4 Pulse capability

The VS3 Power Supply shall continuously monitor and communicate to PCS its status with respect to the capability of providing a full-performance VDE current pulse.

9.10.3.5 Operation outside of design operating space

VS3-PS shall allow PCS to generate current pulses even when the capacitor bank is not fully charged or with a higher than specified repetition rate. Nonetheless the pulse may be aborted as soon as the DC Link voltage has decreased to the predefined minimum value or in case of the protection functions (such as overtemperature) triggers.

9.10.3.6 Degraded performance

The VS3 Power Supply shall communicate to PCS any change in performance level, for instance due to component failures, thermal issues or loss of services such as cooling water, for the purpose of adapting the control to reduced performance of the system or to anticipate failure. The extent to which VS3-PS can provide such information will be agreed during the execution of the Task Agreement and while the design progresses.

9.10.3.7 Control signals from PCS to VS3-PS

The VS3 Power Supply shall accept two setpoint-related signals from PCS, at a continuous and synchronous rate of 1 kHz: (1) the setpoint value and (2) the requested operating mode, being closed-loop voltage control or closed-loop current control. The transition between the operating modes shall be immediate and seamlessly within the limits of control.

9.10.3.8 Time-out mechanism

The VS3 Power Supply shall comprise a time-out mechanism (e.g. watchdog) that resets the power supply output voltage and current setpoints to zero in case no new setpoints have been provided by PCS for a configurable interval, in all Operation states. This function shall be coordinated with the relevant interlock functions.

9.10.3.9 Documenting protection mechanisms

The DA shall provide an exhaustive description in the design documentation of all protection mechanisms incorporated in VS3-PS, including all associated protection threshold levels, in order to allow PCS to perform real-time state estimation of the protections (e.g. $I^2 \ast t$ integral value) for limiting/tripping avoidance purposes.

9.10.3.10 Simulation model

The DA shall develop and provide a simplified simulation model that takes into account the various performance limitations, for deployment in plasma simulation software. The simulation environment (e.g. MATLAB/Simulink, PSIM, Spice) will be agreed during the execution of the Task Agreement.

9.10.3.11 Characterisation of VS3-PS operating space

Irrespective of the performance requirements specified in section 6.1, the DA shall characterise the actual operating space (output performance) of VS3-PS. As a minimum, the following characteristics shall be determined and documented:

1) Continuous RMS output current level
   a. With and without concomitant VDE / Generic pulsed operation
   b. Constrained by VS3-PS limits alone, and constrained by VS3-PS + interfaces
2) Generic pulsed operating capabilities
   a. Maximum pulse duration over the pulse current (RMS)
   b. Recovery time before a subsequent full-performance VDE pulse can be supplied

9.10.4 Central Safety System (CSS-O, PBS 48.02)

To be defined, in accordance with the evolutions of the HIRA at each design gate.

9.10.5 Protocols and Standards

The protocols and standards used to interface with the Central I&C systems are mentioned in Figure 9-17.

The "plug & play" protocols and standards are natively supported by the ITER Central I&C systems and networks. The "possible" interfaces require additional measures to interface with the ITER Central I&C.

Interfacing with CODAC (CCS) – Protocols and Standards

PON	TCN	DAN	SDN
• EPICS • OPC UA • NTP for low precision time	High precision time: • PTPv2 (for low precision time PON)	Network streaming on DAN via CCS library functions	SDN data published / subscribed on SDN via CCS library functions
• Profinet	• pulse per second • TSN	Any timestamped structured data via streaming, e.g. • Shared memory	• Profinet Class C • TSN • Any RT capable network protocol

Possible (with conversion / adaptation with gateway)

Plug & play

Figure 9-17: Protocols and Standards interfacing with CODAC (CCS)

The DA shall state the protocols and interfaces used in interfacing the central I&C systems and networks for all the I&C components foreseen in the technical solution.

In case *Possible* interface standards and protocols are foreseen, it shall be clearly stated if the interfacing will be:

a) Out of scope of the offered solution, and it will be the scope of IO to provide the full integration with ITER I&C by providing the additional measures, or

b) Part of the offered solution implemented by a subcontractor with the relevant experience and track record to provide the additional measures, or

c) Implemented within the scope of the Task Agreement by acquiring the required skills and know-how by the DA to provide the additional measures.

In case "plug & play" interfaces will be used, the DA shall provide evidence of existing skills and know how, or a plan of how to acquire the required skills and know-how of the ITER I&C protocols & standards, the development environment, and tools & processes.

9.11 Building 13 (B13, PBS 62)

The VS3 Power Supply will be installed and integrated in Building 13 – Assembly Hall, part of PBS 62.13.

The VS3 Power Supply shall be designed taking into account all applicable requirements included in the Interface Sheet between PBS 41 and PBS 62.13 [AD88]. The design should take into consideration all relevant information in said document.

The fire loads introduced by VS3-PS in Building 13 shall be minimized, in particular in relation to the ESCB.

The Interface Sheet IS-41-62.13-001 [AD88] records, among other requirements, the installed masses, heat loads and fire loads. The DA shall provide all necessary data to allow IO, in

accordance with the update responsibilities defined in Table 9-1, to update the IS with the most recent values of the agreed interface parameters, including but not limited to masses, heat loads and fire loads.

The following subsections highlight some of the main requirements and supplement the interface requirements in the interface documents.

9.11.1 Presentation of the VS3-PS area

The VS3-PS components shall be installed in the dedicated main steel structure (refer to section 7.10) inside Building 13 and fixed on the B13 slab at level L1.

The VS3-PS will be installed in the north-west of B13. The VS3-PS steel structure is shown conceptually in Figure 9-18.
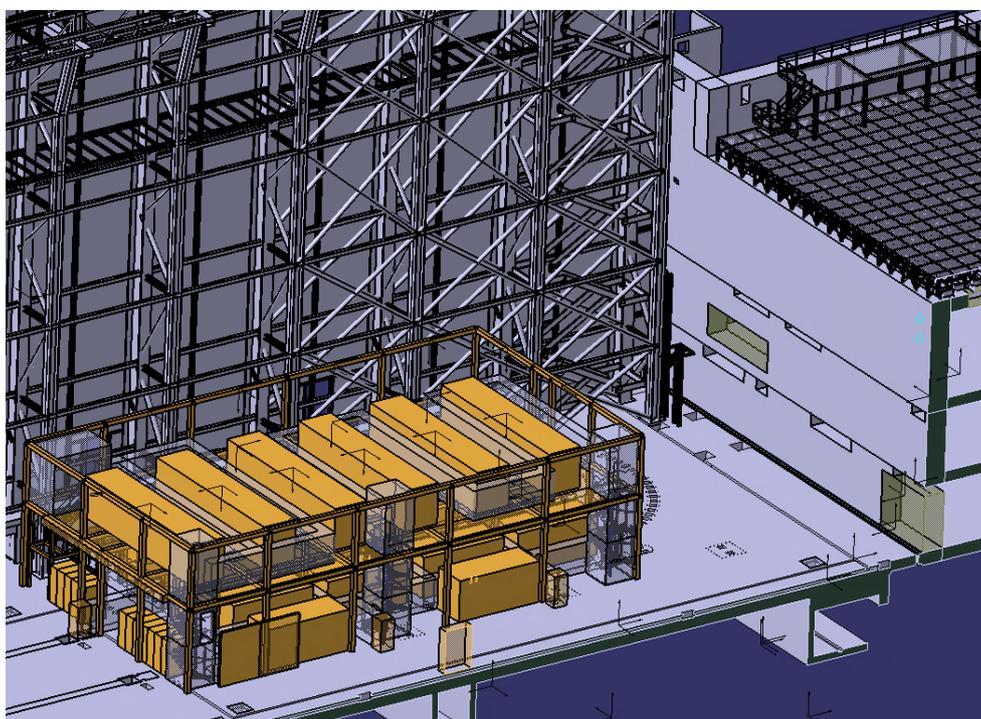
Figure 9-18: global view of VS3-PS in the north-west area of Building 13

9.11.2 Anchoring of VS3-PS components

The existing base supports for the fixation of the VS3-PS components in B13 is the B13 concrete slab at level L1.
As the slab was previously used by other ITER systems, the DA shall perform a site mapping of the concrete slab and make sure the fixation solution designed is in accordance with the actual status of the concrete slab.

The technical solutions used for the fixation of the VS3-PS components shall be removable at any time if required and the initial state of the existing base support shall be recoverable.

The DA shall use post-drill in the B13 concrete slab or use the existing anchors of the Sector Sub-Assembly Tools (SSATs). The two options are further detailed in below subsections.

9.11.2.1 Post-drill in the B13 concrete

The characteristics of the B13 concrete slab are the following:
- Reinforced concrete C40/50
- Thickness 1200 mm

Because the area was previously used by PBS 22, it is highly recommended that DA performs a global inspection (visual, scan or virtual reality if possible) of the future location of the VS3-PS installation in B13 in order to identify any defect of the slab that might jeopardize a correct post-drilling.

This recommendation is motivated by the fact that unrecorded actions like in Figure 9-19 were observed at other locations in B13 where anchors were cut flush to the slab.

Figure 9-19: area in B13 slab with existing post-drill anchor cut flush to the slab

The DA may fix components by implementing Post Drill Systems (PDS), which within the ITER Project is defined as a fastening system meant to be installed after the concrete works are complete.

A PDS assembly is composed of the following items as shown in Figure 9-20:
- Pre-drilled Plate
- Post Drilled Anchors (PDA) (eventually supplemented by Annular gap infill products based on applicable requirements)
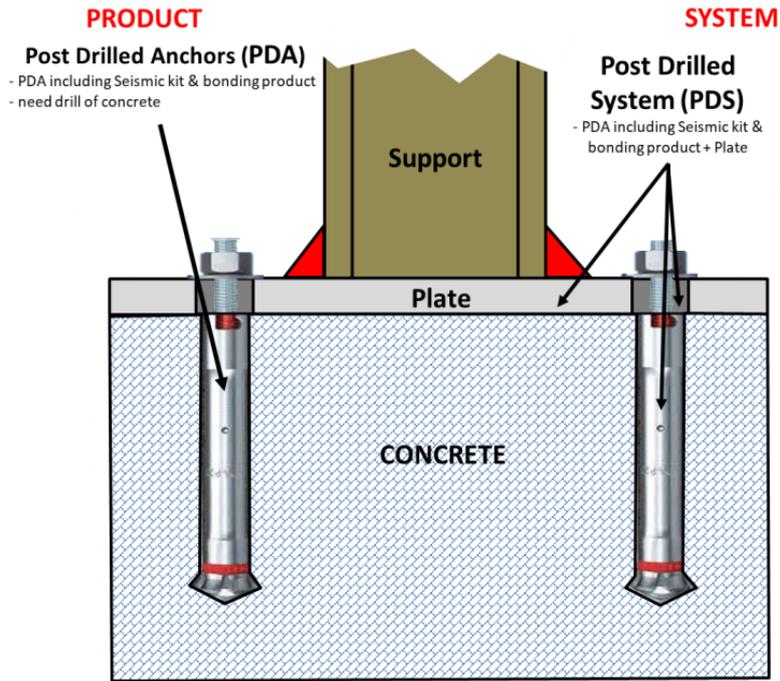
Figure 9-20: PDA & PDS representation

The implementation of a Post Drill Anchor requires drilling activities to be carried out in the frame of the PDA installation process for the which the following requirements apply:
The DA shall size and implement PDSs as per [AD94].

9.11.2.2 Fixation using existing anchors
The location where the VS3-PS will be installed was originally prepared and designed for the SSAT assembly tools as shown in Figure 9-21.
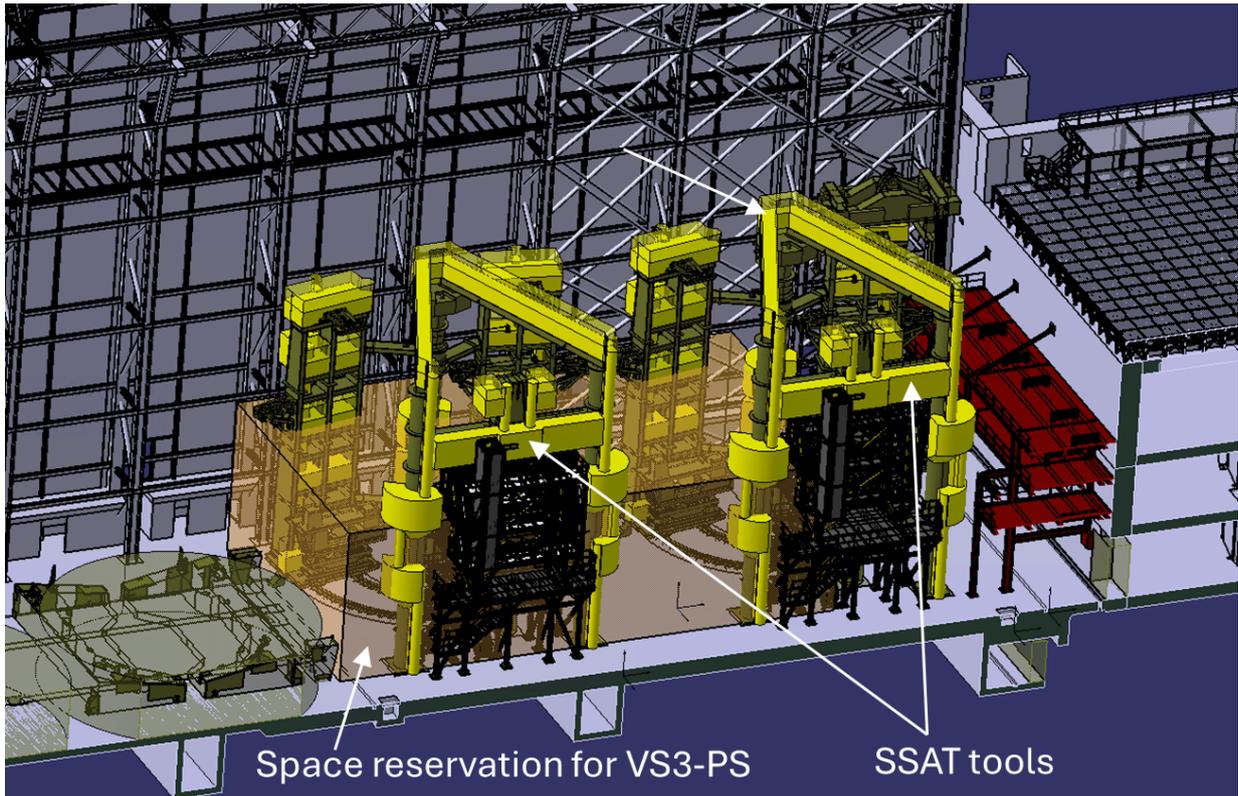
Figure 9-21: view of current (SSAT) and future (VS3-PS) systems occupying north-west area of B13

The SSAT tools will be completely removed to permit the installation of the PBS41.V3 components. But it is foreseen that in the future the reinstallation of one of the SSAT tools may be requested. In that case, all the PBS 41.V3 components will be dismantled and removed, and the SSAT will be re-installed.

The assembly tools are anchored on the B13 with permanent anchoring systems as shown in Figure 9-22.
There are three types of existing anchoring systems designed for the fixation of the SSAT tools, which are identified A, A1 and A2. These anchors may be used by DA for the fixation of VS3-PS, on the condition that no permanent damage is made that would prevent the future reinstallation of the SSAT. The available existing anchor systems are further detailed in Appendix A.
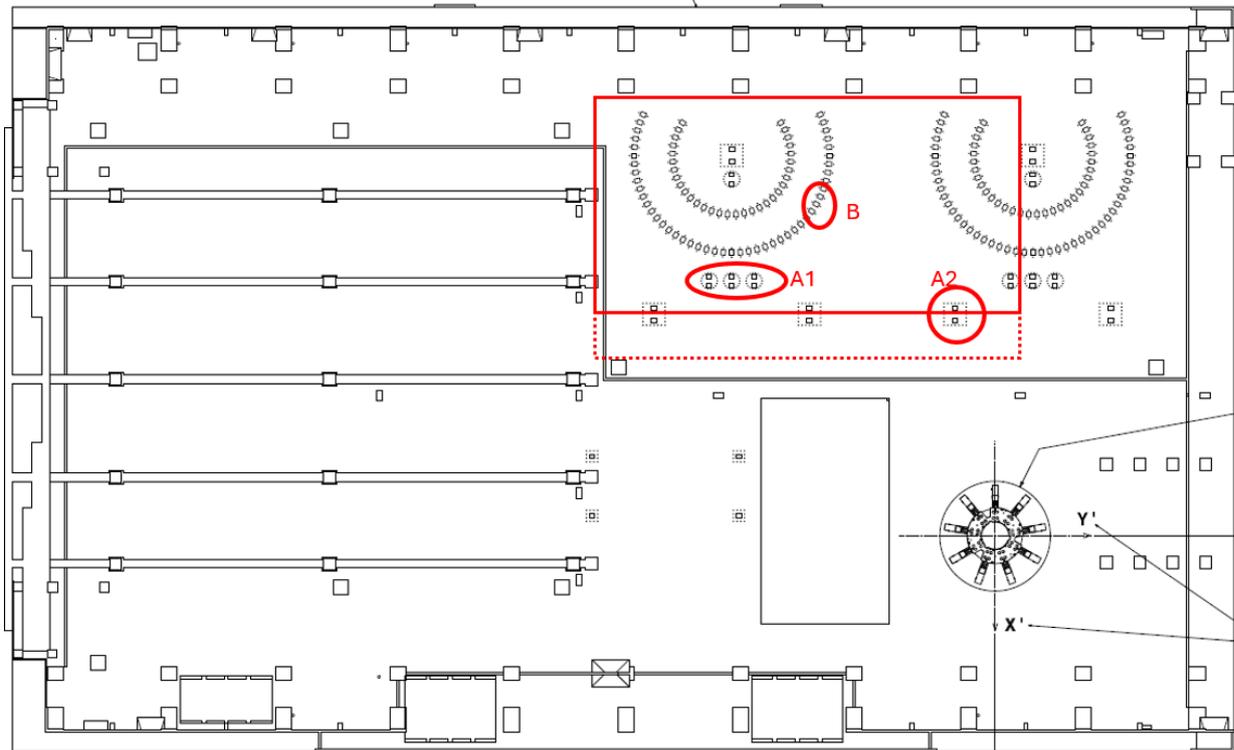
Figure 9-22: locations of existing anchors in B13

9.11.3 Drainage System in Building 13

An Industrial Drainage System is available in B13 for the evacuation of wastewater from B13. The drainage canalization is an open canalization realized in the B13 concrete. The dimension of the existing canalization is:

- Width: 205mm
- Depth: 270mm

The water is evacuated from the canalization to the outside of the B13 by pipes DN100 embedded in the B13 slab.

The closest canalisation of IO's existing Industrial Drainage System in B13 is presented in Figure 9-23 and Figure 9-24. The distance between the canalization and the VS3-PS is approximately 1200 mm. The coordinates of the potential interface point with the Drainage System are:

- X-TGCS: -6510.527mm
- Y-TGCS: -90124.109mm
- Z-TGCS: -1480mm
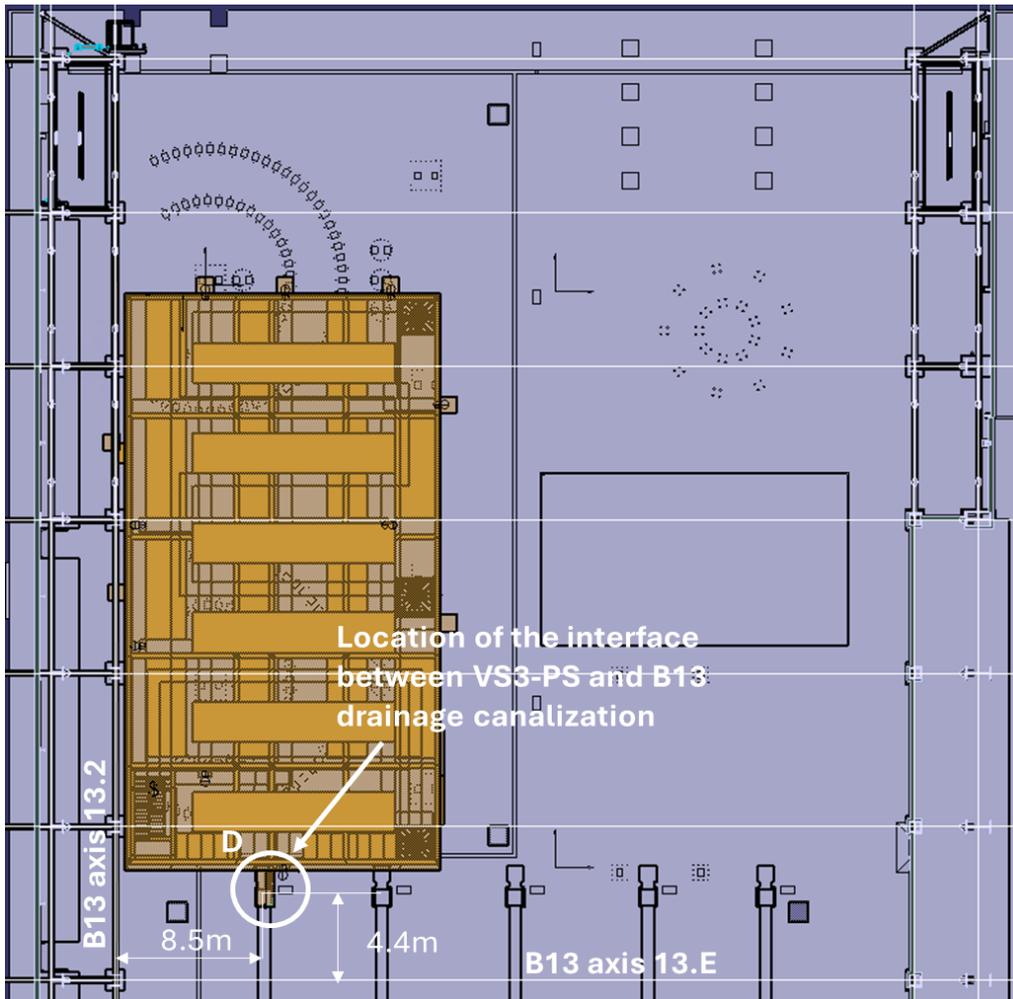
Figure 9-23: location of the drainage canalization in B13
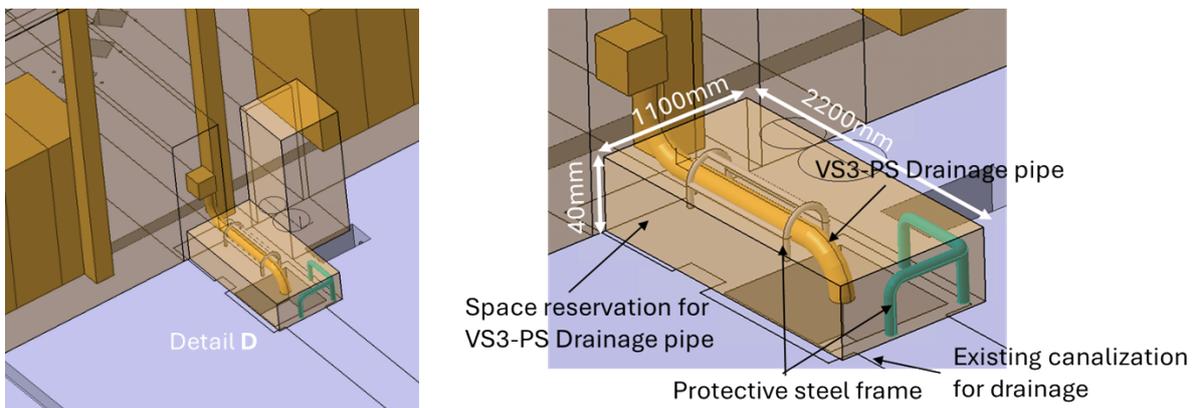
Figure 9-24: potential interface point with IO's Industrial Drainage System in B13

The DA may use this existing wastewater Drainage System in B13 for discharging their water, if any. In that case:

- the entire drainage installation from the VS3-PS system until the existing IO's Industrial Drainage System is DA responsibility

- the DA shall comply with the requirements of the IO's Drainage System on the quality of the wastewater that will be specified at later stage

- the DA shall use all means to contain the wastewater in the canalization and to avoid splashing at the collection point
- the DA shall supply and install all necessary protections for the pipework against damage by e.g. forklifts

The technology to ensure the conveyance of the water inside the pipes is the responsibility of the DA. Currently gravitational conveyance is foreseen.

10 Integration and Environmental Requirements

10.1 Integration in Building 13

The VS3-PS will be installed in Building 13 – Assembly Hall. The internal dimensions of the B13 building are approximately 51m x 97m x 48m.

The B13 building is a common building hosting several other systems. The presence of other systems shall be considered during the installation duties. This will be clarified in the dedicated documentation.
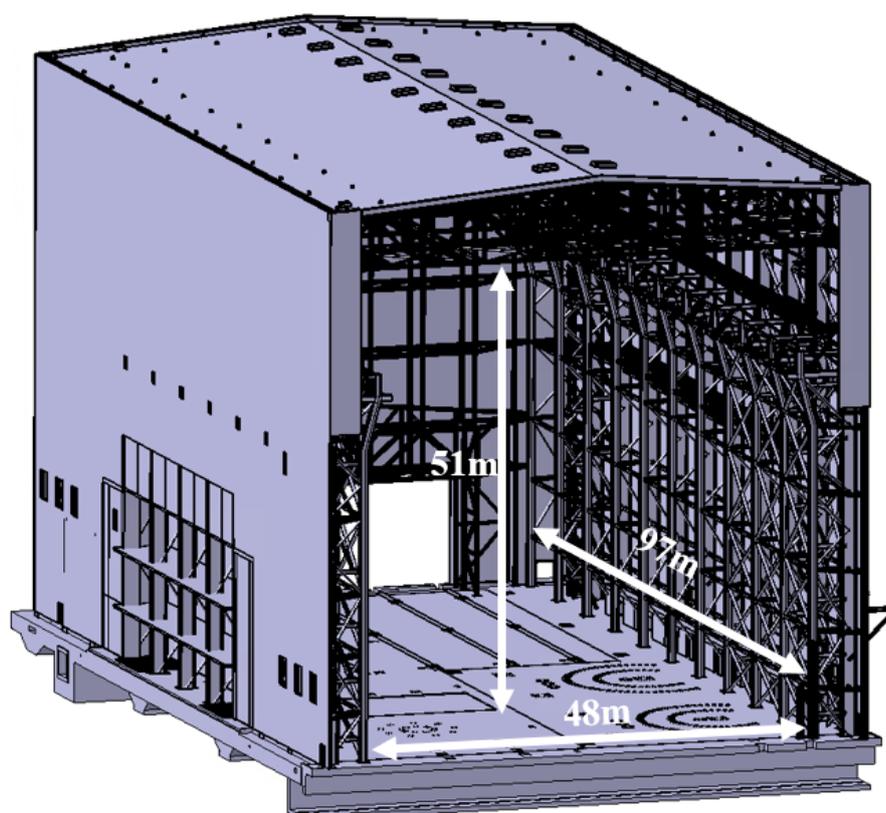
Figure 10-1: impression of Assembly Building (Building 13)

10.1.1 Coordinate System

10.1.1.1 Directions

The axes/directions of this coordinate system are: radial, toroidal, and vertical. The identifier of the toroidal angle is φ counterclockwise when viewed from above. Also, the directions "poloidal" and "toroidal" are often used for load directions, see Figure 10-2.
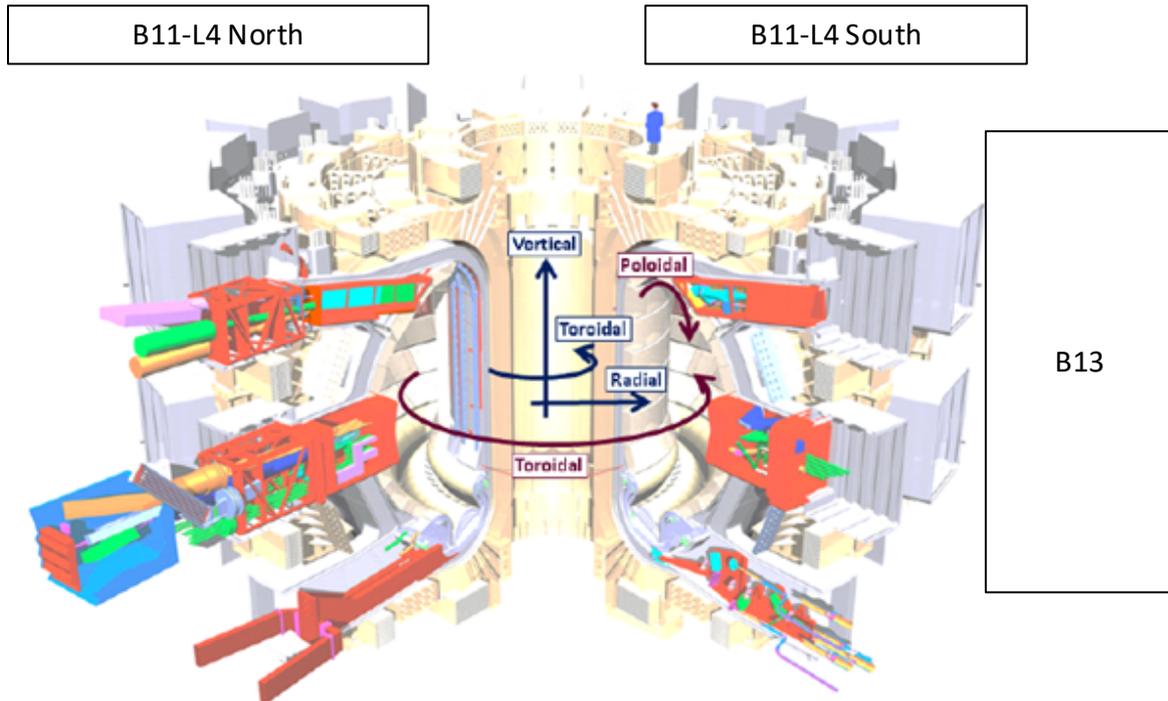
Figure 10-2: ITER Tokamak reference directions

The Magnetic Field Map Database Query Tool User Manual [AD91] and the latest version of the associated tool, which provides the Static Magnetic Field values, use these coordinates since the magnetic field is predominantly generated in radial and vertical directions.

10.1.1.2 Tokamak Global Coordinate System

The Tokamak Global Coordinate System (TGCS) is used to define the location of components at ITER, as detailed in [AD71]. Its origin is at the center of the Vacuum Vessel as shown in Figure 10-3 and Figure 10-4.
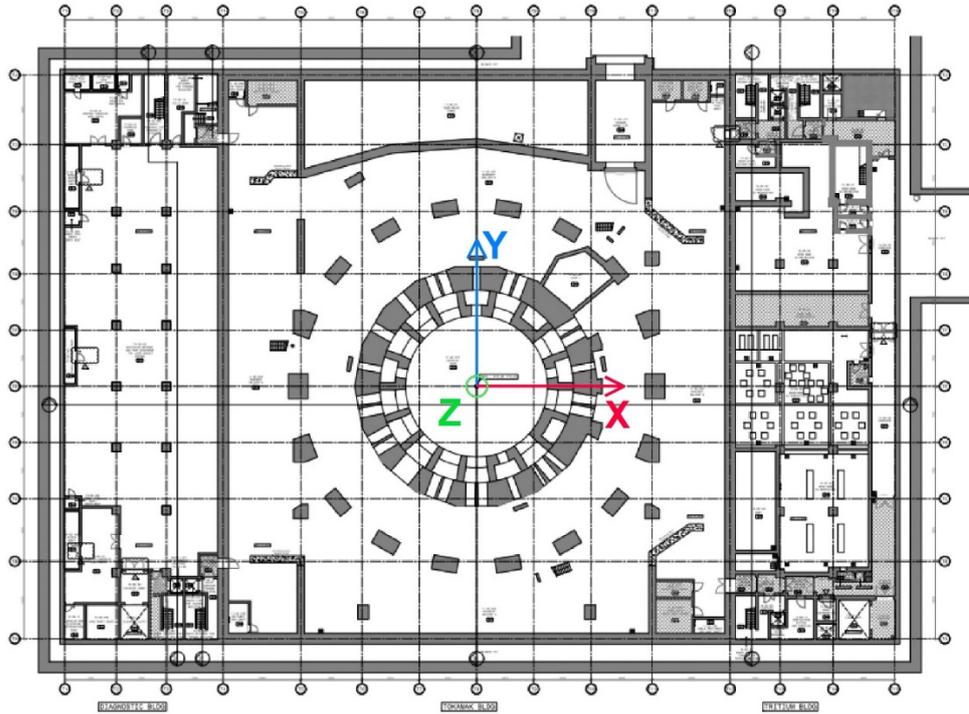
Figure 10-3: Tokamak Global Coordinate System - TGCS (top view)
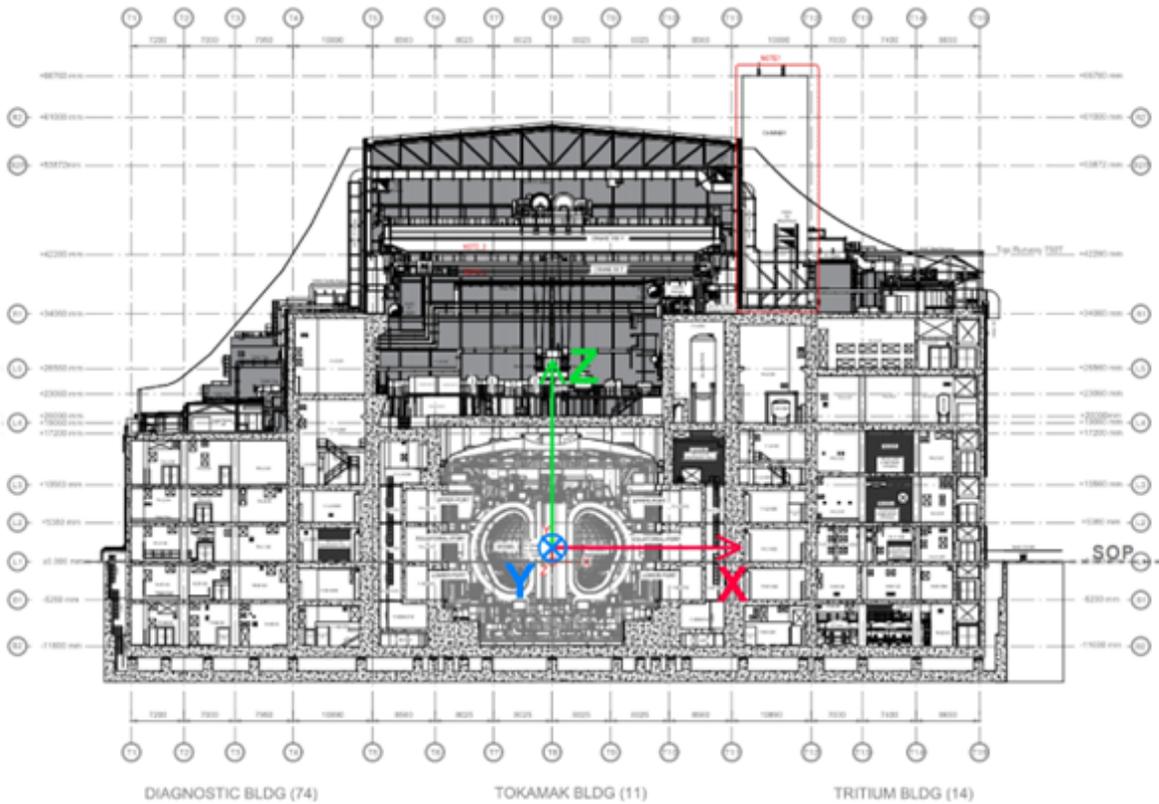
Figure 10-4: Tokamak Global Coordinate System - TGCS (side view)

The origin of all 3D models produced to integrate systems and components in Building 13 shall be defined in accordance with the TGCS.

The TGCS shall be used for the development of models, drawings and for analysis used to integrate VS3-PS SSCs in the respective building(s).

The design of VS3-PS shall equally adopt the definitions of polarity and reference directions in [AD72] in relation to the connection of the VS3 coil circuit to the power supply, and in relation to any integrated analyses where applicable.

10.1.2 Space reservation and environment

The currently approved 3D Configuration Management Model (CMM) of the VS3-PS system is provided in [AD89] with the ENOVIA tree shown in Figure 10-5.
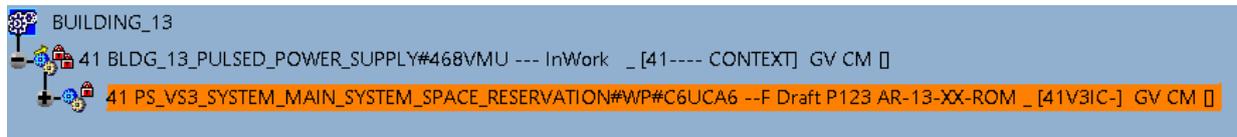
Figure 10-5: ENOVIA links of the VS3 Power Supply in B13

The VS3-PS is to be installed in B13 at approximately 600mm from the axis 13.2 and 4800mm from the axis 13.J, as per Figure 10-6. The CMM takes precedence over these values and this figure.
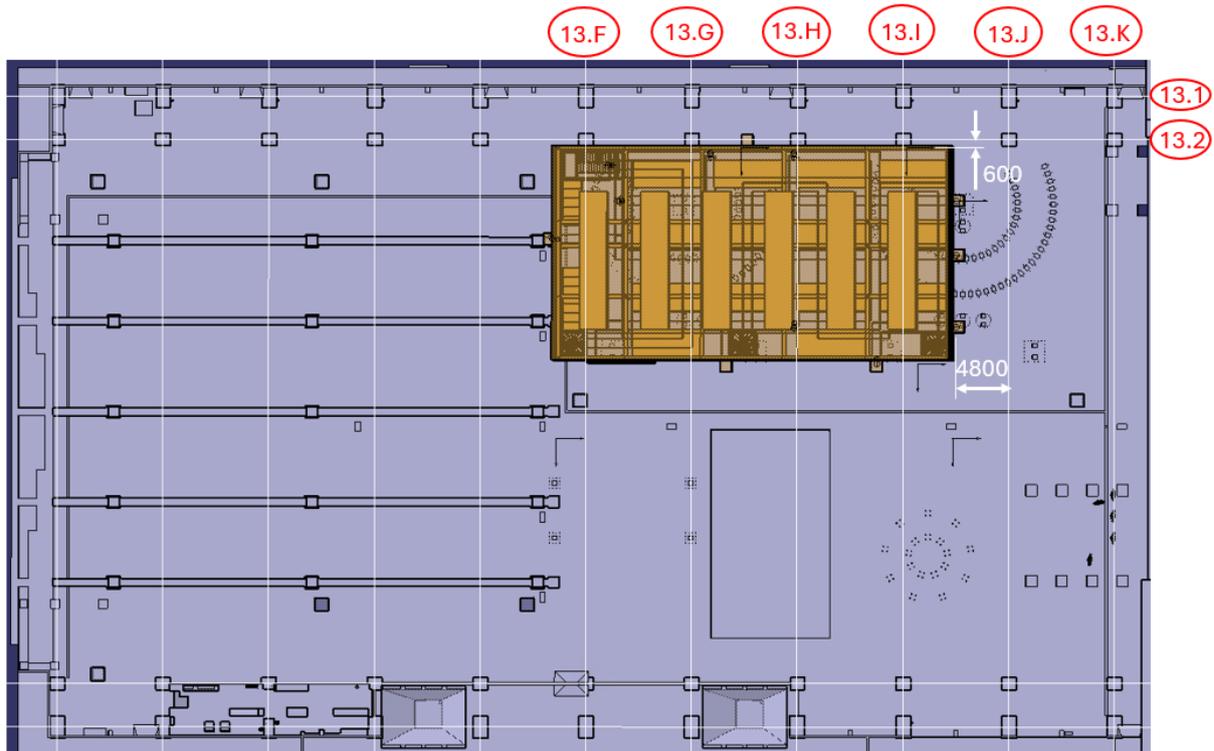
Figure 10-6: Space reservation for VS3-PS in Building 13

The footprint of the VS3-PS space reservation is 665m2, comprised of a length of 35 meters and a width of 19 meters. The reserved height is 11 meters. Figure 10-7 shows the details.

The VS3-PS shall occupy the entire reserved footprint in the CMM; refer to section 7.10.1.
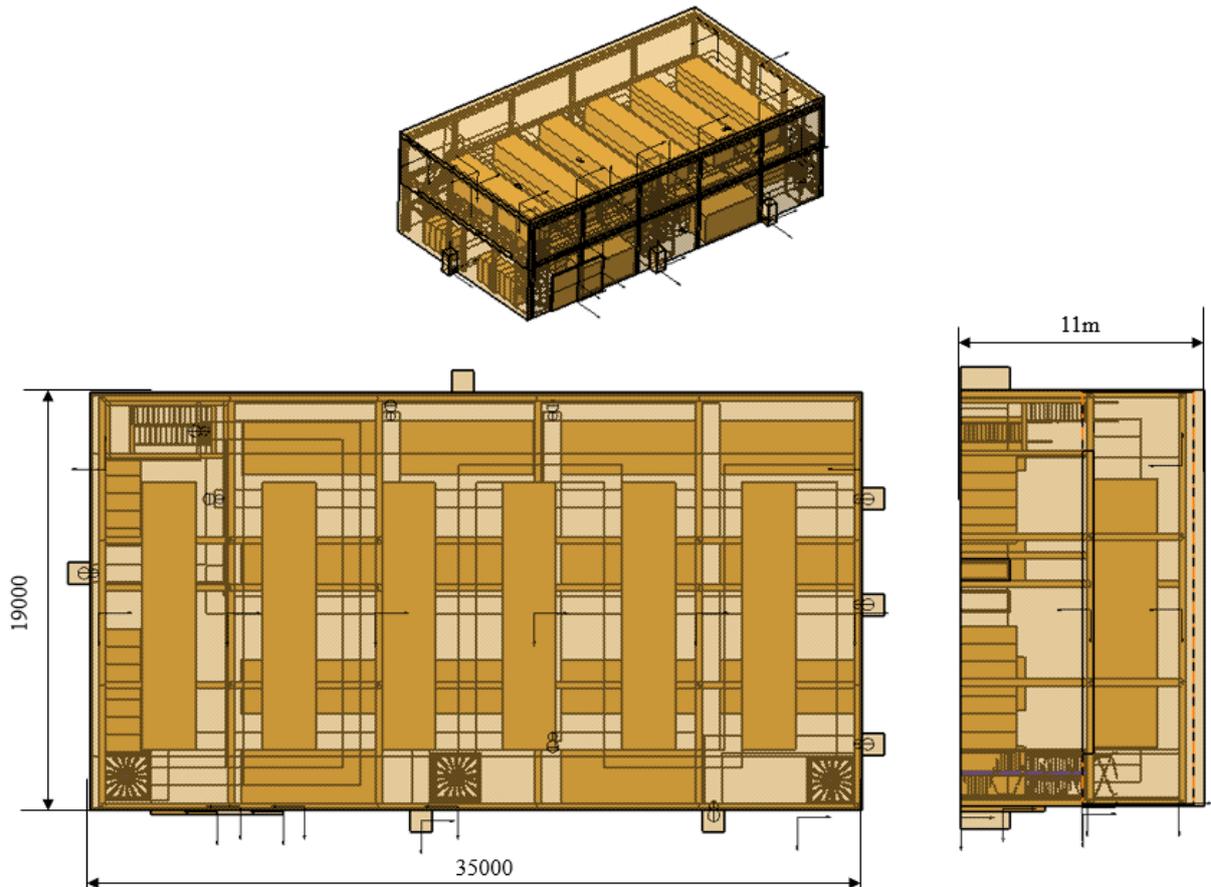
Figure 10-7: dimensions of the VS3-PS space reservation

10.1.3 Fixation of components

The fixation of VS3-PS structures and components on the B13 slab is described in section 9.11.2.

The fixation shall be performed in such a way that the structures and components can be dismounted with reasonable efforts in case required.

10.1.4 Environmental conditions

The environmental conditions in B13 during the operation of the VS3-PS system are summarized in Table 10-1.

Table 10-1: ambient conditions in Building 13

Maximum temperature	35 °C
Maximum humidity	70 %
Pollution degree	Equivalent to PD1 as per IEC 60664-1

10.2 Load Specification

10.2.1 Definition

The VS3-PS Load Specification [AD38] is an applicable document that defines all the loads (mechanical, climatic, thermal, electromagnetic…) that are applied to the VS3-PS system, in the following situations:

- Normal operating situations
- Incident situations
- Emergency situations
- Accidental situations

The Load Specification is an input to the design process and shall therefore be completed and approved before the start of any design activity.

The Load Specification defines two types of loads:

1. External loads, which are applied on the VS3-PS system by other systems or external conditions and events (seismic, ambient conditions in the B13, fire in B13, stray magnetic fields produced by the TKM machine, etc). These loads are already defined by IO in the load specification [AD38].
2. Internal loads generated by the VS3-PS system (masses, internal (electro)magnetic fields, heat, etc.).

The DA shall define all internal loads of the VS3-PS system.

The applicable load specification for the design of VS3-PS is provided in [AD38].
The DA shall develop the load specification for VS3-PS as per [AD50], [AD39] and [RD42].

The loads currently defined in [AD38] shall be considered and supplemented where required and updated load specification(s) shall be approved by IO once all internal and external loads are defined and integrated by DA. For that purpose:

- The responsibility to update the load specifications will be handed over to the DA.
- If necessary, separate load specifications can be created for specific subsystem(s).

10.2.2 Seismic loads and Floor Response Spectra

Since the VS3-PS SSCs are classified SC2, the following seismic loads shall be considered:

- SL-1
- SMHV
- SL-2

10.3 Electromagnetic Compatibility

10.3.1 Static Magnetic Field compatibility

Due to the proximity of the B13 with the tokamak building, some components of VS3-PS may be subject to a Static Magnetic Field greater than 5 mT. Above this threshold, specific requirements in terms of qualification and design shall be determined. The magnitude of the Static Magnetic Field (SMF) for the components located in B13 is shown in Figure 10-8, for information - the values in the Magnetic Field Map Database Query Tool [AD91] take precedence.

All VS3-PS equipment located in B13 or in close vicinity of the Tokamak complex shall be designed to operate reliably in the presence of stray magnetic fields provided in Static and Transient Magnetic Field Maps in Tokamak Building [AD90], the most recent values of which can be obtained through the Magnetic Field Map Database Query User Manual [AD91] and associated Tool.
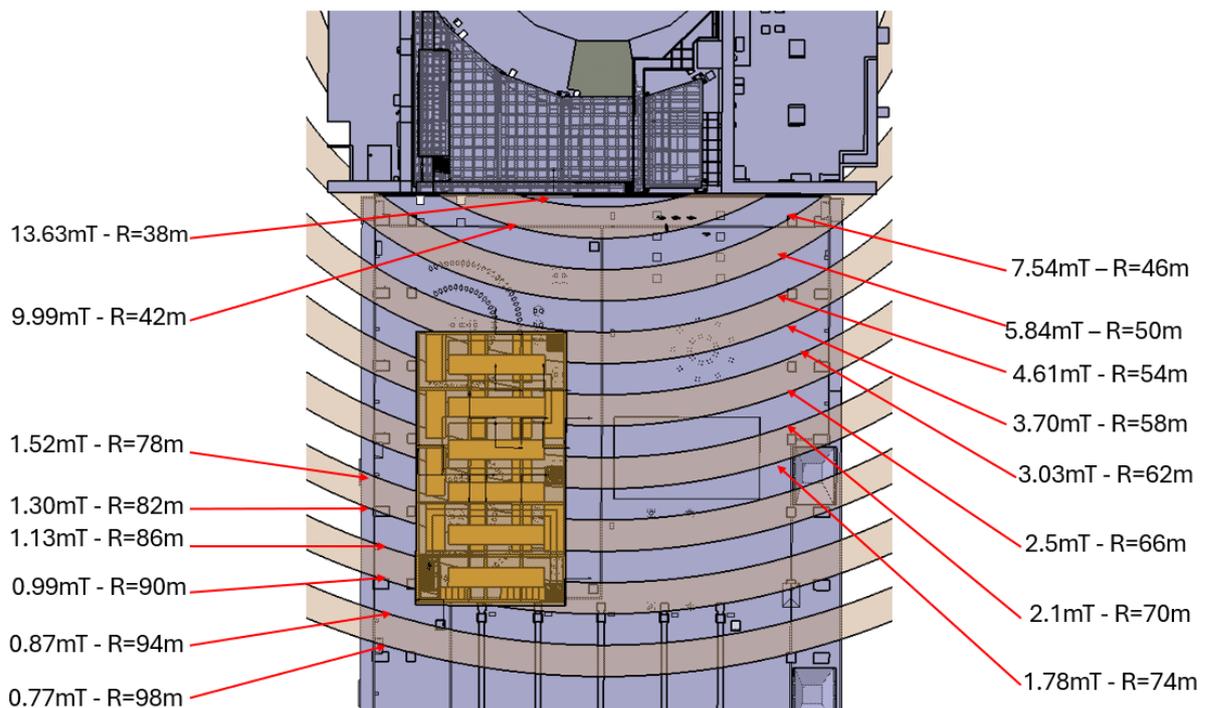
Figure 10-8: magnitude of the stray magnetic field in B13, obtained using [AD91]

10.3.2 Electromagnetic Interference

The design of the power system shall prevent any mains network disturbance or mutual interference with any other system connected to the mains. The VS3 power converters and control system shall satisfy the following standards:
- Noise emission (E.M.I.) according to IEC 61204-3, class B limits for input and output,

- Electrical fast transient/Burst immunity test according to IEC-61000-4-4 on all the cables (AC, DC, controls) and control system,
- Electrical surge immunity test according to IEC-61000-4-5 on all the cables (AC, DC, controls) and control system.

All VS3-PS equipment shall be designed to operate reliably in the presence of stray electromagnetic fields that are self-generated by the VS3-PS equipment, such fields including those generated during short-circuit conditions.

Entryways to areas with stray magnetic fields greater than 0.5 mT shall be marked with appropriate signage.

10.4 Integration, space, access and circulation

The DA is responsible for the integration of the VS3-PS system in Building 13.

The general rules, in terms of space for circulation, maintenance and operation are defined in [AD73]. The space for circulation, operation and maintenance can be also imposed by technical aspects like the size of spare components to be removed/brought from/to the VS3-PS system, the tools used for maintenance and other aspects. Consequently, the requirements in [AD73] shall be considered as minimal requirements.

10.5 Assembly and disassembly requirements

The VS3-PS system shall be designed in such a way that it can be assembled and dismantled with limited effort and time. For that purpose:

1) Bolted or clamped assemblies are preferred at the interface points with buildings, false floors, etc.

2) The systems, assemblies, cabinets, components, etc. shall be designed in a modular way, to reduce the duration of assembly and dismantling phases, e.g. as per section 8.5.

3) The modules of the modular design shall encompass complete functions as much as possible, e.g. rectifier modules, inverter modules, ESCB modules, etc.

4) All structures, assemblies and cabinets shall be designed and equipped with the necessary hardware to allow for lifting with standard lifting tools (slings or similar).

11 Occupational Safety Requirements

11.1 Occupational safety management and requirements

11.1.1 IP ratings

All the VS3-PS subsystems and/or internal electrical components shall have an IP rating of IP2X or better. This requirement equally applies to components inside the cabinets.

Particular attention shall be taken to ensure the correct temperature inside the enclosures.

MV components and MV rooms may be subject to more stringent requirements, as imposed by the NF-C 13-200 [CS24].

standard.

11.1.2 Sound Pressure Levels (SPL)

Dielectric breakdowns and arc flash events involving the Energy Storage Capacitor Bank may result in considerable sound and pressure waves that could be harmful to nearby workers. For the design of the VS3-PS, strict adherence to the French labour Code is required regarding the exposure limit values of noise, particularly peak values.

The peak Sound Pressure Level (SPL) resulting from an arc-flash event shall be limited by design to 135 dB(C) at any location outside of the VS3-PS space reservation. Inside the VS3-PS space reservation, the peak SPL shall not exceed 137 dB(C).

11.1.3 Hazard Identification and Risk Assessment (HIRA)

Before each design gate review (i.e. PDR and FDR), the Hazard Identification and Risk Assessment report (HIRA) shall be updated [RD32].

The HIRA report specifies the minimum safety level to be reached. If any mitigation measures are to be changed, e.g. due to technical constraints, an equivalent level of safety shall be ensured by the alternative measures.

The HIRA report is an integral part of the Input Data Package of each design gate review.

The update of the HIRA report is the responsibility of IO, nevertheless the DA shall provide all necessary and up-to-date information for this purpose.

11.2 Electrical risks

The following standards shall be considered for the design, installation and operation of the VS3-PS system:

1. NF C 15-100: Low-voltage electrical installations.
2. NF C 13-200: High voltage electrical installations.
3. NF C 18-510: Operation of electrical installations - Prevention of electrical risk

If required, IO will involve an independent third party to check the compliance with these standards during the design phases.

Regulatory inspections of the VS3-PS system will be performed at different stages to ensure the correct implementation of the standards, as defined in section 15.2.

11.3 Compliance with standards and French national regulations

Before the start of the commissioning activities, the DA shall provide a technical dossier and certificate(s) that prove that the VS3-PS system and its components have been designed, manufactured and implemented in accordance with the NF C 15-100 [CS25] and NF C 13-200 [CS24] standard and/or articles R4215-1 to R4215-17 of the French Labor Code.

The certificates are binding for the DA and engage their responsibility.

For low voltage electrical components, the CE marking of the components and subsystems should be the first option to comply with this requirement, since it addresses the requirements of the articles R4215-1 to R4215-17 of the French Labor Code.

The second option is to testify that the VS3-PS system components were designed, manufactured and implemented as per the NF C 15-100, NF C 13-200 and their applicable standards.

The DA shall define the content of the technical dossier with the third party that will perform the regulatory inspections.

12 Nuclear Safety Requirements

12.1 General requirements

12.1.1 Non-aggression

Operation, inadvertent actuation or damage to the VS3 Power Supply System, shall not prevent Safety Important Component (SIC) systems, structures, or components from accomplishing their safety functions when required.

The function of a Hardened Safety Core Component (HSCC) shall not be jeopardized by the failure of the VS3 Power Supply.

The DA shall demonstrate that the VS3 Power Supply cannot aggress components classified as PIC, including but not limited:
-   Building 11 concrete structure and penetrations
-   IVC busbar penetrations at B11-L4 (refer to section 12.2)
-   IVC feedthroughs (refer to section 12.2)
-   Cable trays containing SIC trains

In addition, the Building 13 structure shall not be damaged in case of collapse of VS3-PS SSCs.

The requirement of non-aggression is applicable to explosion and over-current for all VS3-PS system modes, states and configurations.

The justification of non-aggression in case of collapse will be managed by IO.

The exhaustive list of PIC components to be considered for compliance with the non-aggression requirement shall be established during the execution of the Task Agreement.

12.1.2 Explosion

Under any design conditions (normal, incidents, accidents, aggressions and combinations) and including the application of the single failure criterion, the VS3-PS shall be designed, operated and maintained in order to prevent explosion to occur.

12.2 Current limits for IVC Busbars and VS coil components

The VS3 Power Supply System is electrically connected to the IVC busbar with penetrations through the B11-L4 slab and to the VS coil feedthroughs (PBS 15.IV), both of which are classified as PIC.

The DA shall demonstrate, and provide all necessary justifications in the framework of nuclear safety, that the maximum current supplied by the VS3 Power Supply to the VS3 coil circuit – in all possible configurations and under all load combinations and relevant failure modes – is inherently limited to **95 kA** by design.

For the purposes of this requirement, 'by design' shall be understood to mean that the limit is impossible to be exceeded by the laws of physics and without reliance on any active component or any form of physical actuation.

The justification may be based on the parasitic inductances and resistances, the finite energy in the capacitor bank, the multiple layers of independent and diverse protection mechanisms, the operational independence of the power converters, etc.

The justification documentation shall include a comprehensive fault scenario identification and fault current calculation report.

The final justification shall undergo independent peer review.

In the event that such justification cannot be provided, the VS3-PS Crowbar System shall be classified as PIC and the design, qualification, manufacturing, delivery, storage and installation shall be performed accordingly.

13 Design and Design Process requirements

The DA shall organize design reviews in liaison with the IO in accordance with the requirements given in "Design Review Procedure (2832CF)" [AD21].

The Manufacturing Readiness Review shall be performed by the DA in accordance with "Working Instruction for Manufacturing Readiness Review (44SZYP)" [AD25].

Mandatory Gate Reviews required by IO in the implementation of this TA and their associated Hold Points, together with other reviews, are listed in this Technical Specification. The expected content and the maturity at each design gate of typical deliverable documents developed as part of the System Design is described in "Expected content of System Design deliverables (43S7GL)" [AD24].

Design interfaces shall be managed according to "Design Interface Control Procedure (28VNJG)" [AD33].

The DA shall ensure that analyses and calculations shall be performed in line with the "Procedure for Analyses and Calculations (22MAL7)" [AD41] and related Instructions listed in "General Management Specification for Service and Supply (82MXQK)" [AD1].

Both physical items and items identified in Drawings shall be labelled according to the "Procedure for Identification and Controls of Items (U344WG)" [AD30] and "ITER Numbering System for Components and Parts (28QDBS)" [AD31].

13.1 System Design Process

The DA shall take the responsibility of performing the preliminary design, final design, manufacturing design and preparation for the VS3-PS system. They shall follow Design Development Procedure [AD22], ITER System Design Process (SDP) Working Instruction [AD23], and MQP L3 Expected content of System Design deliverables [AD24] to complete the design and pass the corresponding design reviews, as required by Design Review Procedure [AD21].

After the design process, the DA shall be responsible for performing the manufacturing, FAT, delivery, site installation and assembly, SAT and commissioning on dummy load, following the instructions and requirements, such as those specified by the ITER Quality Assurance Program [AD6].

13.1.1 TA design and development plan

Based on the applicable IO requirements and procedures, the DA shall prepare a TA design and development plan which includes description, requirements, plan, schedule and material/documentation deliverables for the key activities in each TA stage.

13.1.2 Schedule

The DA shall also develop a schedule for their activities covering all the tasks within the TA and submit this document for review and acceptance, initial version to be reviewed at the KOM. The DA will show in their schedule all the key activities and tasks to cover their full scope, including but not limited to:
- Milestones;
- TA Gates;

- Design and analysis activities;
- R&D and prototyping;
- Procurement and sub-contracting activities if any;
- Manufacturing Preparation, Manufacturing and Assembly;
- Factory Acceptance Tests;
- Delivery;
- Site installation preparation and installation activities;
- Site Acceptance Tests preparations and SAT tests.

The schedule for documentation deliverables is covered by the Document Schedule as integral part of the TA.

13.1.3 Interfaces

During all the TA stages (in particular the design stages), the DA shall be responsible to manage the interfaces with other systems, with the support from IO, in accordance with the Working Instruction for Interface Management [AD34]. This responsibility includes but is not limited to:

- Respecting the interface constraints
- Ensuring the design meets the interface requirements
- Updating the interface control documents in accordance with maturing of the design and up to the final as-built data

13.1.4 Document deliverables

All the document deliverables shall be managed in accordance with the following requirements:

- all document deliverables shall be uploaded into IDM with the original format (Word, Excel, Visio, etc), and respect the ITER Sign Off Authority [AD37]
- the design analysis shall be provided with analysis models (circuit simulation models and FEM models)
- all CAD deliverables shall be produced and managed in accordance with the applicable CAD working instructions (section 13.6).

13.2 Preliminary Design

The key activities, input and output for this stage are defined in the following table:

Table 13-1 Preliminary Design Activity Phase: inputs, outputs and objectives, adopted from [AD23] and supplemented

Preliminary Design Activity Phase (PRE)	
Phase Inputs	• Technical specifications covering consolidated Technical/Engineering data produced by IO during the Conceptual Design phase • Forward Workplan (Design Plan and DPP for the PRE phase)

Main Objectives	• To produce the documents for the considered system (PBS node) scope and maturity relevant for the Preliminary Design Activity phase as indicated in the Document Production Plan (DPP).
	
	 • At the beginning of the Preliminary Design Activity phase, to select a design option if various solutions were defined during Conceptual Design
	
	 • To refine the Conceptual Design in order to confirm the technical feasibility and the robustness of schedule. Evidence is given in:
	
	  o An update of the Design Description (DDD) with detailed set of schematics and carefully considering margins and contingencies.
	
	  o Functional Diagrams (P&ID, SLD, I&C architecture, etc)
	
	  o An update of the System Load Specification [AD38]
	
	  o An update of the definition justification documents, referring to a first consistent set of justification notes demonstrating that the technical objectives of the systems requirements will be met (analyses, return of experience, tests, simulations) and that manufacturability, transfer, assembly and qualification/start-up of the system have been addressed
	
	 • To allocate system requirements to the participating subsystems (in s-SRD) in order to comply with the general architecture of the system.
	
	 • Support analysis and calculations
	
	 • To complete Interface specifications (assumptions, ranges, actual data) once the level of detail of the design allows the production of Interface Sheets (IS) and relevant Configuration Management Models (CMMs) and room book,
	
	 • To plan the future steps of justification in a consistent way (in particular all the tests on mock-ups/prototype for design qualification/verification should be planned in Verification/Qualification Plan)
	
	 • To re-assess the technical risks of the selected solution and provide mitigation plan before going to the detailed design (Risk/Hazard Analysis Report [RD18][AD55], RAMI Analysis Report, HIRA Report)
	
	 • To check that the proposed design solution definition still meets the RQs (DCM/VCM for SRD and s-SRD)
	
	 • Provide documents required according to Design Review Procedure 18[AD23] and MQP L3 Expected content of System Design deliverables [AD24]

Phase Outputs (Maturity Level)	System Design with the preliminary design maturity: • General architecture (Functional: FBS, Physical PBS-GBS) is consolidated and the main (or critical) components described adequately. • All Interface Requirements shall be fully defined. All the IS should be agreed (as evidenced by their approved status) and defined either by a fixed value or by allocation of ranges. • Functional Specifications and outline drawings of assy/loops (PBS level 3) are available with their traceability matrices. • Configuration Item (CI) Level 3 are identified according to the identification of items defined in [AD23][AD30] • Preliminary I&C analysis and design report as defined in PCDH [AD46]

This Phase is terminated with the acceptance of the Close-out Report of the Preliminary Design Review (PDR).

13.3 Final Design

The key activities, input and output for this stage are defined in the following table:

Table 13-2 Final Design Activity Phase: inputs, outputs and objectives, adopted from [AD23] and supplemented

Final Design Activity Phase (FIN)	
Phase Inputs	• Technical/Engineering data produced during the PRE phase • Workplan (Design Plan and DPP for the Final Design Activity phase) *The plan shall clearly define the scope (system i.e. Configuration Item Level 1 or Level 2) and the boundaries, especially if the scope is smaller than previous phase (Preliminary design).*

Main Objectives	• To produce the documents for the considered system (PBS node) scope and maturity relevant for the Final Design Activity phase as required per applicable design procedure and indicated in the Document Production Plan (DDP).
	• To refine the design to a level where the final definition of the product (PBS element) is sufficiently complete to allow starting the manufacturing design & preparation phase (subsystem/component specifications are detailed enough to be "understandable" by the manufacturer) – in particular the Engineering-BOM and a preliminary Manufacturing-BOM are available
	• To update all ICD/IS according to refined design definition
	• Updated analysis and calculations used for design justification
	• Updated spare part list and management strategy
	• To have a complete and approved CMM (under config branch)
	• To have completed all R&D activities with the associated prototype design reports and test reports (items, procedure, results). Prototyping and test activities are expected for at least the following components:
	    o Main power transformer (if non-COTS),
	    o ESCB cells,
	    o Customized fuses (if any) for capacitor and converters,
	    o Rectifier / inverter module,
	    o Crowbar
	    o Current & voltage sensors for regulation and protection purpose,
	    o Dummy load
	• To build a complete set of justifications demonstrating that:
	    o Component specifications and design are justified (supporting analyses, return of experience, tests and explanations)
	    o The specification of the qualification process is fixed (test objectives, logical sequencing, expected results, etc.)
	    o The manufacturability, transfer, assembly and qualification/start-up of the system are defined and agreed with the stakeholders

	• To develop documentation covering the following aspects of the system: manufacturability, on-site delivery, assembly/installation, commissioning, operation and maintenance of the system • To provide all documents required according to Design Review Procedure 18[AD23] and MQP L3 Expected content of System Design deliverables [AD24], including but not limited to updated versions of FMECA, HIRA, and RAMI reports, a preliminary integration plan (including site test procedure) and a preliminary SAT plan.
Phase Outputs (Maturity Level)	Plans for next phases (manufacturing, installation, commissioning, operation and maintenance) • Complete definition of the system (DDD, diagrams, 3D models (DM/CM), drawings, component lists, etc) • Detailed definition of the composing PBS elements (i.e. Functional References) ready for manufacturing/detailed design. • Full set of justification documents (including DCM, Structural Integrity Reports, etc) • Plans for next phases (manufacturing, installation, commissioning, operation and maintenance) • Updated I&C analysis and design report as defined in PCDH [AD46]
Note	Considering the high energy storage capacity of the ESCB and the associated electrical risks and both component and VS3-PS system level, the DA shall provide sufficient justification in this stage that the DA is able to build/develop the technical solution meeting the technical, interface and safety requirements. This shall be done by prototyping and testing of the key components at full scale, including at least one ESCB cell undergoing a short-circuit test under representative conditions.

This Phase is closed with the acceptance of the Close-out Report of the Final Design Review (FDR), giving the Authorisation-to-Proceed (ATP) to the next activity phase (Manufacturing Design and Preparation).

13.4 Manufacturing Design, Preparation and Manufacturing

The key activities, input and output for this stage are defined in the following table:

Table 13-3 Final Design Activity Phase: inputs, outputs and objectives, adopted from [AD23] and supplemented

Manufacturing Design & Preparation Activity Phase	
Phase Inputs	• Detailed definition of the composing PBS elements (Functional References) ready for manufacture studies, • Workplan (Design Plan and DPP for the Manufacturing Design and Preparation Activity phase). *The plan shall clearly define the scope (system i.e. Configuration Item Level 1 or Level 2) and the boundaries, especially if the scope is smaller than previous phase (Final design).*
Main Objectives	• To produce the documents for the considered scope and maturity relevant for the Manufacturing Design and Preparation Activity phase as indicated in the Design Plan.

	• To refine the design definition (Manufacturing Design) to a detailed level for the workshop execution (manufacturing drawings, fabrication, factory acceptance tests, data sheet for COTS, Manufacturing and Controls procedures, Weld Plan, tooling, trainings, materials certificates, tagging procedure)
	
	• To generate Manufacturing-Bill of Materials (M-BOM) and deliverable list.
	
	• To generate a Procurement Plan for COTS and materials
	
	• To generate Manufacturing Implementation Plan (MIP).
	
	• To build a complete set of justifications demonstrating that:
	   o Manufacturing design is compliant with the Manufacturing requirements (Compliance Matrices - VCM),
	   o Manufacturing Design is justified (supporting analyses, return of experience, tests and explanations),
	   o Component Qualification is finalised (in particular for PIC)
	   o Manufacturing processes are qualified

Phase Outputs (Maturity Level)	Manufacturing design: • Manufacturing Inspection Plan • Detailed definition of the composing products/equipment's and their identification following [AD30], ready for procurement (for COTS) or actual fabrication. • Detailed definition of the welded joints (welding maps…) • Material certificates • Manufacturing Procedures, NDT procedures, tagging procedures • Factory Acceptance Test Plan and procedures, • Qualified manufacturing, coating and assembly processes and tools • Qualification of operators • Requirements for the preservation of the product and its qualification over the product lifecycle.

This Phase is closed with the acceptance of the Close-out Report of the Manufacturing Readiness Review (MRR), giving the Authorisation-to-Proceed (ATP) to the next activity phase (Manufacturing).

After the MRR, the DA shall adhere to the procurement plan to procure the necessary raw materials and COTS, and the Manufacturing Implementation Plan to perform the manufacturing activities.

A MIP is required and section 8.4.2 [AD1] shall be applied. If deemed appropriate, multiple MIPs may be produced instead of a single one, with one MIP per subsystem/component.

MIPs shall list all operations that are critical from a quality point of view. As such, QARO and IO TARO reserve the rights to request for MIP revision if any activity considered critical is not listed in MIPs. MIPs shall be subject to acceptance by IO.

13.5 Design and Simulation Tools

13.5.1 Analyses and calculations

The DA shall apply Procedure for Analyses and Calculations [AD41] as well as all lower level Instructions, Templates and Checklists made applicable by the Procedure.

The instructions, templates and checklists for structural, seismic, electromagnetic and Computational Fluid Dynamics (CFD) analyses are summarized in section 7.2 of the GM3S [AD1].

Structural, seismic, electromagnetic, computational fluid dynamics analysis should be performed following the procedures, templates, reviewer checklists, etc. defined in section 7.2 of the GM3S [AD1]. For other types of analysis, unless specified otherwise, no specific requirements are imposed but the instructions provided in [AD41] shall be followed.

Structural Integrity Reports shall be developed in accordance with the requirements in [AD41]. Guidance for meeting these requirements is provided in the Guideline for Structural Integrity Report [RD30].

13.5.2 Software qualification

Any software used for R&D, design, manufacturing, installation, construction, commissioning, or operation of the VS3 Power Supply shall be qualified in accordance with the Software Qualification Policy [AD42] to ensure its quality and integrity prior to approval for use. The qualification shall be undertaken to demonstrate that the software adequately and correctly performs all intended functions and meets all user requirements.

The DA is encouraged to use the following software, which is already qualified and implemented at IO:

-   For transient simulations of electrical systems: MATLAB/Simulink, PSIM or PLECS
-   For electrical power distribution analysis: Caneco
-   For 3D Finite Element Analysis: Ansys software (including the electromagnetic desktop)
-   For structural analysis: Ansys, GTStrudl, STAAD or ROBOT
-   For piping analysis: CAESAR II and/or PIPESTRESS
-   For RAMI and FMECA analysis: Reliasoft

The use of other software is possible under the following conditions:

-   qualified in accordance with the Software Qualification Policy [AD42], and
-   commercially available for use at IO, and
-   approved by IO prior to its use

13.5.3 Source files

All source files generated used for R&D, design, manufacturing, installation, construction, commissioning, or operation of the VS3 Power Supply shall be provided by DA to IO.

13.6 Computer Aided Design (CAD) requirements

The following requirements apply in relation to Computer Aided Design activities and outputs:

a) All diagrams, models and drawings are subject to the Procedure for the CAD management plan (2DWU2M) [AD75].

b) The DA shall exchange CAD data relevant for the design and associated interfaces with the IO in the CAD software and related versions indicated in the latest revision of the ITER CAD Manual (CAD Manual 01 - Instruction for Use and Introduction (AHFDDK) [AD53]) released by the Design Office of the IO.
CAD data may be exchanged in other formats if compatible with the IO software and if agreed by the IO through the DCIF associated to this TA. The DA shall ensure compliance with this requirement, including for the CAD data issued by its Suppliers.

c) The DA shall ensure that all CAD Data (Schematics, 3D Models, Drawings, derived engineering data, etc.) prepared by the DA, or its Suppliers, comply with the Design Collaboration Implementation Form (DCIF) for the Design activities related to the Procurement of the VS3 Power Supply:
[DCIF - 41 - TA - XXXXXXXXX - ITER VS3 Power Supply (Design, Manufacturing, Test, Installation and Commissioning) (FPMACN)](#)

14 Welding Requirements

14.1 Welding requirements for pipes

This section specifies the welding requirements for pipes part of the VS3-PS cooling water network including the interface with PBS 26.CC.2A. Pipes implemented inside cabinets (rectifiers, inverters, transformers, etc.) and welds of components that are water-cooled (heatsinks, heat exchangers, etc.) are not concerned.

14.1.1 Weld classification for pipes

For pipes that are designed based on the EN codes and standards, the quality levels given in Table 14-1 shall be considered.

For pipes that are designed following ASME codes and standards, the ASME B31.3 shall be considered.

Table 14-1: weld classification for pipes designed based on EN codes and standards

Quality level	
Limit of imperfection (EN ISO 5817)	C
Execution class (NF EN 1090-2)	EXC2

14.1.2 Welding process for pipes

The welding process for pipes shall be executed following the EN or ASME reference standards listed in Table 14-2.

Table 14-2: codes for the welding of pipes

Components designed under EN codes	Components designed under ASME codes
EN 13480-4 EN 13480-5 EN 13480-6 EN ISO 15614 ISO 9606 EN ISO 17635	ASME B31.3 ASME BPV

In addition, the following requirements apply.
   a) Peening is not allowed to repair welds.
   b) Imperfections and defects shall be removed.
   c) Repairs of welds shall be tested with Non-Destructive Testing (NDT).
   d) Temporary attachments shall be removed by cutting and/or grinding (not by hammering).
   e) Attachment welds to pipe shall be continuous.
   f) An examined item with one or more defects shall be repaired or replaced; the repair shall be re-examined using the same methods, extent and acceptance criteria as the original work.

14.2 Welding requirements for structural components

The welding requirements included in this section apply to welds that ensure the mechanical and structural integrity.

14.2.1 Weld classification for structural components

For structures and structural components designed according to EN codes, the quality levels stated in Table 14-3 shall be considered.

Table 14-3: weld classification for structures and structural components designed based on EN codes and standards

Category	Description	Quality level	
		EN ISO 5817	NF EN 1090-2
		Limit of imperfection	Execution class
Structural components ensuring safety of people	Welds that ensure the structural integrity	B	EXC3
	All other welds	C	EXC2
All other structural components	All welds at attachment points with the base supports, e.g. the welds on the post-drill plates, the welds on the main steel structure in B13.	B	EXC3
	All other welds	C	EXC2

For structures and structural components designed according to ASME codes, the requirements given in the codes and standards stated in Table 14-3 shall be considered.

Table 14-4: weld classification for structures and structural components designed based on ASME codes and standards

Material	Applicable code
Carbon steel	AWS D1.1/D1.1M:2008
Stainless steel	AWS D1.6/D1.6M:2007

14.2.2 Welding process for structural components

The welding process for structures and structural components shall be executed in accordance with the codes and standards listed in Table 14-5.

Table 14-5: codes and standards for the welding of structures and structural components

For components designed with EN codes	For components designed with ASME codes
EN 1090-2	AWS D1.1
ISO 3834-2	AWS D1.6
EN 544	ASTM E 709
EN 15614-1	ASTM E 165
EN 15614-2	
EN ISO 15609	
EN ISO 15609-1	
EN ISO 15607	
EN ISO 9606-1	
EN ISO 14732	
EN ISO 5817	
EN 1090-2	
EN ISO 5817	
EN ISO 9712	
EN ISO 17637	
EN ISO 5817	
EN ISO 17637	
EN ISO 10042	
EN ISO 3452-1	
EN ISO 23277	
EN ISO17636-1	
N ISO 10675-1	
ISO 17640	
ISO 17641	
ISO 22825	
ISO 23279	
ISO 11666	

14.3 General welding requirements

14.3.1 Welding specification

Before manufacturing, the welding specification shall be provided.

The welding specification describes for each step of the work the methods/processes, material, operators (if required), etc. An example is provided in ITER_D_YPQ82Y.

14.3.2 Traceability

An identification system for materials used in fabrication shall be established (base material and welding consumables), so that each material can be traced to its origin.

The surface condition necessary for performing all Non-Destructive Testing (NDT) shall be in accordance with EN ISO 17635 Appendix A. This includes removing of spatters, slag, scaly oxides, grease etc. liable to interfere with the inspections and NDT.

14.3.3 Surface roughness

The surface roughness shall be smaller than 6.3 after welding.

14.3.4 Welding documentation

Upon completion of all welding, the final welding documentation shall be provided.

The final documentation includes, but not limited to, the following items:

a. As-built isometric and manufacturing drawings (if different than the ones provided before
b. Welding Data Packages (Weld Maps, Weld Log)
c. NDT and other control reports.
d. Welding Procedure Qualification Record (WPQR)
e. Welder and Welding Operators Qualification (WQ) or Welder Qualification Test Record (WQTR)
f. Actual List of Welders & Operators (version applicable during the manufacture)
g. Actual List of NDT inspectors.
h. NCRs related to each component and Deviation Request, if any.

15 Factory Acceptance Testing and Site Acceptance Testing

15.1 General requirements

15.1.1 Requirement Validation

Before the closeout of the TA, the DA shall demonstrate by tests that all requirements are met.

Tests that can only be performed on the actual VS coils, i.e. during integrated commissioning and not on the dummy load, will be executed by IO during integrated commissioning and are not in the scope of DA. However, should such tests reveal any non-compliance with the requirements, the DA shall be responsible for implementing the necessary corrective measures, therefore the DA shall provide support during integrated commissioning.

15.1.2 Reducing on-site activities and risks

The DA shall perform tests on the VS3-PS subsystems or components at the earliest feasible stage and prior to delivery, with the objective of reducing on-site activities and minimizing the risk of failures during the commissioning phases with the associated risk of schedule delay.

15.2 Regulatory inspections

Regulatory inspections are requested by the French law and focus on electrical risks and personal safety. The regulatory inspections shall be conducted based on the NF C 15-100 [CS24], NF C 13-200 [CS25] and NF C 18-510 [CS26] standards.

In case of non-conformities, the DA should implement the eventual corrective actions before starting the next activity and reflect the modifications all affected documents.

The approach of early inspections (i.e. off-site and shortly after installation) is adopted to identify non-conformities at an early stage and to enable the DA to implement corrective actions as soon as possible, thereby mitigating the risk of schedule delay.

Note: only the final regulatory inspection prior to system energization is mandatory, and will be performed by an independent third party. The off-site and post-installation inspections are strongly suggested but optional, and may be performed by an IO staff member or an independent third party.

15.2.1 Off-site inspections

Regulatory inspections should be carried out on the components/subsystem listed hereafter, taking advantage of the modular architecture, prior to delivery to IO:

    a) First unit of the VS3-PS rectifier stage
    b) First unit of the VS3-PS inverter stage
    c) First unit of ESCB module
    d) First unit(s) of LV cabinet(s) (if applicable)
    e) First unit(s) of I&C cabinet(s) (if applicable)

15.2.2 Post-installation inspections

Regulatory inspections should be performed at the IO site, shortly after the installation of the components/subsystem listed hereafter, before starting testing activities:

  a) VS3-PS rectifier stage (including transformers and auxiliary systems)
  b) VS3-PS inverter stage
  c) ESCB module(s)
  d) DC Link
  e) Mechanical switches
  f) Crowbar system
  g) Metallic structure (if applicable)
  h) LV and I&C cabinets (if applicable)

15.2.3 Pre-energization regulatory inspection

Regulatory inspections shall be performed on the installed VS3-PS system at the IO site and prior to the system commissioning stage.

This approach is proposed to identify non-conformity and to allow the DA to implement corrective actions as soon as possible for avoiding schedule delays.

15.3 Factory Acceptance Tests

The detailed FAT plan, comprising test procedures and acceptance criteria, shall be defined by the DA during the manufacturing design phase for IO's acceptance, as per design process requirements (refer to chapter 13).

The FAT plan shall comprise as a minimum all tests specified in the relevant standards, e.g. [CS1], [CS2], and define the acceptance criteria based on standards, operating conditions, requirements and industrial best practices.

The following sections list the minimum tests to be performed and shall be supplemented by DA where required for the final FAT plan.

15.3.1 System tests and tests common to multiple subsystems

15.3.1.1 Full power tests

The VS3 Power Supply shall be factory-tested at full voltage, full current and at full operating power.

15.3.1.2 Visual inspection

Acceptance criteria:

  1) No damage or deterioration of the subsystem or components after the manufacturing and the FAT.
  2) Basic technical requirements and dimensions of the components meet all the specified design requirements.
  3) Internal components are correctly labelled and identified.
  4) Internal components are correctly fixed on the structure.

15.3.1.3 Wiring check

Acceptance criteria:

1) The subsystem or components has been implemented and wired as in the schematics and manufacturing dossier.

15.3.1.4 Auxiliary devices check

The operation of the auxiliary devices such as contactors, pumps, sequencing equipment, fans, etc., should be checked according to

Reference: clause 7.5.1 of IEC 60146-1-1 or equivalent

Acceptance criteria:

1) During and after the test, it shall be verified that all the auxiliary devices are operating properly.

15.3.1.5 Cooling water circuit pressure drop

The hydraulic pressure drop of all subsystems interfaced with the cooling water system shall be measured.

The test shall be conducted at the factory ambient temperature (5°C ~ 40°C), with water passing through the circuit at the specified nominal flow rate, and with all components (pipes, hoses, fittings, manifolds, gauges, etc.) of the cooling circuit assembled substantially as they would be when they are introduced into service, as far as features affecting the test result are concerned.

Acceptance criteria:

1) The measured maximum pressure drop satisfies the design requirement

15.3.1.6 Cooling water circuit tightness

The cooling water circuit shall be pressurized at the specified test pressure level (1.5 times the rated pressure for 1 hour), with the inlet pipe connected to a pressure pump and the outlet pipe fully blocked.

Acceptance criteria:

1) The connection, joints and terminations show no evidence of leakage.

15.3.2 VS3-PS power transformer (part of rectifier stage)

As part of the FAT of the VS3-PS Power Transformer, the DA shall perform the tests listed in Table 15-2 (minimal list) and demonstrate that acceptance criteria are met.

Table 15-1: minimum type and routine tests to be performed on the VS3-PS power transformers

Test Items	Type Test	Routine Test	Reference
Visual inspection	X	X	
Wiring checking	X	X	Section 15.3.1
Checking of auxiliary devices	X	X	

The tightness test of the water-cooling circuit	X	X	
Measurement of the pressure drop	X		
Measurement of winding resistance	X	X	This section
Measurement of voltage ratio and check of phase displacement	X	X	
Measurement of short-circuit impedance and load loss	X	X	
Measurement of no-load loss and current	X	X	
Separate-source AC withstand voltage test	X	X	This section
Induced AC withstand voltage test	X	X	
Lightning impulse test	X		
Partial discharge measurement	X	X	This section
Temperature-rise test	X		
Short circuit tests	X		

15.3.2.1 Measurement of winding resistance (routine test)

This test shall be performed as per clause 10.2 of IEC 60076-1 standard or equivalent.

Acceptance criteria:

1) The windings resistances are consistent with the requirements and the planned performance.

15.3.2.2 Measurement of voltage ratio and check of phase displacement (routine test)

This test shall be performed as per clause 10.3 of IEC 60076-1 standard or equivalent.

Acceptance criteria:

1) The voltage ratio and phase displacement are consistent with the requirements or the planned performance.

15.3.2.3 Measurement of short-circuit impedance and load loss (routine test)

This test shall be performed as per clause 10.4 of IEC 60076-1 standard or equivalent.

Acceptance criteria:

1) The short-circuit impedance and load loss are consistent with the requirements or the planned performance.

15.3.2.4 Measurement of no-load loss and current (routine test)

This test shall be performed as per clause 10.5 of IEC 60076-1 standard or equivalent.

Acceptance criteria:

1) The no-load loss and current are consistent with the requirements or the planned performance.

15.3.2.5 Separate-source AC withstand voltage test (routine test)

The test shall be performed as per clause 19 of the IEC 60076-11 standard or equivalent.

Acceptance criteria:

1) During and after the tests, there shall be no damage to the transformer and no insulation failures

15.3.2.6 Induced AC withstand voltage test (routine test)

The test shall be performed as per clause 20 of the IEC 60076-11 standard or equivalent.

Acceptance criteria:

1) During after the tests, there are not damage and no insulation failure on the transformer.

15.3.2.7 Lightning impulse test (type test)

The test shall be performed as per clause 21 of the IEC 60076-11 standard or equivalent.

Acceptance criteria:

1) During after the tests, there are not damage on the transformer and there is no insulation failure.

15.3.2.8 Partial discharge measurement (routine test)

The test shall be performed as per clause 22 of the IEC 60076-11 standard or equivalent.

Acceptance criteria:

1) The partial discharge level is consistent with the planned value and the performance requirements.

15.3.2.9 Temperature-rise test (type test)

The test shall be performed as per clause 23 of the IEC 60076-11 standard or equivalent.

Acceptance criteria:

1) The temperatures are consistent with the planned value and the performance requirements.

15.3.2.10   Short-circuit test (type test)

This test is not mandatory if a short-circuit type test has already been conducted on the same transformer model, manufactured using the exact same process and under identical production conditions.

For any transformer design (including manufacturing process) that has not undergone a type test, the short-circuit test shall be carried out as per clause 25 of the IEC 60076-11 standard. Following completion of the short-circuit test, the partial discharge test shall be repeated, and a visual inspection shall be performed.

Acceptance criteria:

1) The temperature of the windings and the isolation material do not exceed the values given in the 60076-5 standard.
2) The transformer (and auxiliary system) has not suffered from mechanical damage.

15.3.3 VS3-PS rectifier and inverter stages

As part of the FAT of the VS3-PS rectifiers and inverters, the DA shall perform the tests listed in Table 15-2 (minimal list) and demonstrate that acceptance criteria are met.

Table 15-2: minimum type and routine tests to be performed on rectifier and inverter stages

Test Items	Type Test	Routine Test	Reference
Visual inspection	X	X	Section 15.3.1
Wiring checking	X	X	
Functional tests	X	X	
Checking of auxiliary devices	X	X	
The tightness test of the water-cooling circuit	X	X	
Measurement of the pressure drop	X		
Insulation tests	X	X	This section
Light Load Test and functional tests	X	X	
Checking the properties of the control equipment	X	X	
Checking the protective devices	X	X	
Rated Current Test	X	X	
Measurement of the inherent voltage regulation	X		
Measurement of ripple voltage and current	X		
Measurement of harmonic currents	X		
Power loss determination for assemblies and equipment	X		
Temperature Rise Test	X		
Power factor measurement (for rectifier only)	X		
Voltage Response Test	X		This section
Test with of I&C subsystem, Mini CODAC & PSH (if possible)	X		
Inverter short-circuit test	X		
Interlock functions tests	X		

15.3.3.1 Insulation tests (routine test)

This test shall be performed as per clause 7.2 of the IEC 60146-1-1 standard or equivalent.

For type tests, the insulation resistance shall be measured as defined in clause 7.2.3.1 of the IEC 60146-1-1 standard.

Acceptance criteria:

1) The acceptance criteria given in clause 7.2 of the IEC 60146-1-1 standard apply.

15.3.3.2 Light-Load Test and functional tests (routine test)

This test shall be performed as per clause 7.3.1 of the IEC 60146-1-1 standard or equivalent.

The VS3-PS inverter and rectifier should be tested at output current levels that correspond to the continuous noise current operation, for a duration of at least 6 hours and until the rectifier/inverters have reached their thermal steady state.

Acceptance criteria:

1) During and after the test, all components and the cooling system of the rectifiers or inverters operate as planned and as specified, without tripping
2) The acceptance criteria given in clause 7.3.1 of the IEC 60146-1-1 standard apply.

15.3.3.3 Checking the characteristics of control equipment (routine test)

This test shall be performed as per the clause 7.5.2 of the IEC 60146-1-1 standard or equivalent.

Acceptance criteria:

1) The acceptance criteria given in clause 7.5.2 of the IEC 60146-1-1 standard apply.

15.3.3.4 Checking the protective devices (routine test)

This test shall be performed as per clause 7.5.3 of the IEC 60146-1-1 standard or equivalent.

Acceptance criteria:

1) The acceptance criteria given in clause 7.5.3 of the IEC 60146-1-1 standard apply.

15.3.3.5 Rated Current Test (type test)

This test shall be performed as per clause 7.3.2 of the IEC 60146-1-1 standard or equivalent.

The output current of the rectifier and the inverter should correspond to their nominal current.

Two different tests should be performed with the dummy load:

a) One with a VDE pulse current profile at full current level (i.e. 3x VDE every 10 seconds)
b) One with the continuous noise current for a duration of at least 6 hours and until the rectifier/inverters have reached their thermal steady state.

The temperature of the semiconductors and the components equipped with temperature sensors that contribute to the overtemperature protection should be recorded and checked.

Acceptance criteria:

1) During and after the test, all components and the cooling system of the rectifier and inverter operate as planned and as specified.
2) The acceptance criteria given in clause 7.5.3 of the IEC 60146-1-1 standard or equivalent apply.

15.3.3.6 Measurement of the inherent voltage regulation (type test)

This test shall be performed as per clause 7.3.4 of the IEC 60146-1-1 or equivalent.

Acceptance criteria:

1) The performance of the rectifier and inverter are consistent with the requirements or the planned performance.

15.3.3.7 Measurement of ripple voltage and current (type test)

This test shall be performed as per clause 7.3.5 of the IEC 60146-1-1 or equivalent.

Acceptance criteria:

1) The performance of the rectifier and inverter are consistent with the requirements or the planned performance.

15.3.3.8 Measurement of harmonic currents (type test)

This test shall be performed as per clause 7.3.6 of the IEC 60146-1-1 or equivalent.

Acceptance criteria:

1) The performance of the rectifier and inverter are consistent with the requirements or the planned performance.

15.3.3.9 Power loss determination for assemblies and equipment (type test)

This test shall be performed as per clause 7.4.1 of the IEC 60146-1-1 or equivalent.

Acceptance criteria:

1) The performance of the rectifier and inverter are consistent with the requirements or the planned performance.

15.3.3.10 Temperature Rise Test (type test)

This test shall be performed according as per clause 7.4.2 of IEC 60146-1-1 standard or equivalent. The temperature of the semiconductors and the components equipped with temperature sensors that contribute to the overtemperature protection should be recorded and checked.

Acceptance criteria:

1) The temperatures of rectifier and inverter and their internal components are consistent with the requirements or the planned performance.

15.3.3.11 Rectifier power factor measurement (type test)

This test shall be performed on the VS3-PS rectifier as per Clause 7.4.3 of IEC 60146-1-1 standard or equivalent.

Acceptance criteria:

1) The power factor is consistent with the specified performance requirements and the planned performance.

15.3.3.12 Voltage Response Test (type test)

This test should be performed with the VS3-PS inverter being supplied by the VS3-PS rectifier and the nominal AC voltage. The test should be performed for different output voltage values, in closed-loop voltage control mode, and under the approximate nominal load impedance of the inverter.

Acceptance criteria:

1) The performance requirements defined in section 6.1 are met.

15.3.3.13 Test of I&C subsystem and Mini CODAC (type test)

The VS3-PS I&C system and the local controller of VS3-PS rectifier and inverter are connected to the mini CODAC. Tests should be performed to check the correct operation of the two systems as per the final implementation in the IO plant.

Acceptance criteria:

1) All signals, exchanged between the local controllers and VS3-PS I&C system shall be individually checked.
2) The integration with Mini CODAC shall be tested as well.
3) The data exchange between the VS3-PS I&C system and the Mini CODAC & PSH shall be functional without loss or corruption of the data or the signal.

15.3.3.14 Inverter short-circuit test (type test)

The inverter shall be subject to a short-circuit type test to qualify the design. The test configuration shall be representative of the operational arrangement and shall be submitted to IO for acceptance. The type test shall demonstrate the correct functioning of all internal protection functions, including, but not limited to, fault detection, current limiting, semiconductor switch gate blocking, and coordinated shutdown. Oscilloscope records of converter currents, voltages, and protection activation times shall be captured and submitted.

Acceptance criteria:

1) The inverter shall be fully protected against short-circuit conditions and shall have no degradation.

15.3.3.15 Interlock functions tests (specific test)

The interlock functions should be tested, when possible, in realistic conditions. The DA shall define the interlock functions to be tested as well as the testing conditions. As a minimum, the following interlock functions shall be tested:

a) Overvoltage protection
b) Overcurrent protections (including short-circuits)
c) Overtemperature protection
d) Capacitors discharge systems

The tests should be performed several times to ensure that the required performance does not change over time.

Acceptance criteria:

1) The interlock functions operate as planned and the interlock requirements are met.

15.3.4 Energy Storage Capacitor Bank

15.3.4.1 Short-circuit test on ESCB cell

Short-circuit tests shall be conducted on the elementary ESCB cell to verify its fault-current interruption capability, to quantify the electrical energy released during the fault, and to demonstrate both the structural integrity of the capacitor enclosures and the absence of damage to the capacitors.

The test conditions and the associated pass/fail acceptance criteria shall be explicitly defined and agreed with IO prior to the execution of any tests.

15.3.5 Crowbar system

The DA shall perform the tests presented in Table 15-3 (minimal list) on the crowbars part of the Crowbar System and demonstrate that acceptance criteria are met.

Table 15-3: minimum type and routine tests to be performed on crowbar system

Test Items	Type Test	Routine Test	Reference
Visual inspection	X	X	
Wiring checking	X	X	
Functional tests	X	X	
Checking of auxiliary devices	X	X	Section 15.3.1
The tightness test of the water-cooling circuit	X	X	
Measurement of the pressure drop	X		
Impulse voltage test	X	X	
Freewheeling switch tests with external triggering	X	X	This section
Short circuit test with self-triggering	X	X	

15.3.5.1 Crowbar tests with external triggering

The crowbar shall be connected to a power source that can provide a current equivalent to the one that will be seen by the freewheeling switches during their operation. The crowbars shall be instrumented to acquire the voltage, current in each branch and the temperature of the main components. The freewheeling switches shall be triggered by the external control system to simulate a short-circuit / overcurrent protection action of the PIS.

Acceptance criteria:

1) The crowbar operates as planned and the interlock requirements are met.
2) The temperature of the components is consistent with the expected values.

15.3.5.2 Crowbar tests with self-triggering

The freewheeling switches shall be connected to a power source that can provide a current equivalent to the one that will be seen by the freewheeling switches during their operation. The crowbars shall be instrumented to acquire the voltage, current in each branch and the temperature of the main components. The control circuit of the crowbar shall not be supplied with an external source. The voltage of at the crowbar terminals is increased until the crowbar self-triggers.

The test shall be executed with two configurations: (1) the control circuit of the crowbar is energized, and (2) not energized.

Acceptance criteria:

1) The crowbar operates as planned and within the expected amount of time

2) The temperature of the components is consistent with the expected values.

15.4 System commissioning

During the commissioning on dummy load, the DA shall demonstrate the compliance with all relevant technical, operational and performance requirements.

Requirements that cannot be fully demonstrated during the commissioning on dummy load phase will be registered and re-evaluated during the integrated commissioning phase.

15.5 Integrated commissioning

Integrated commissioning including the VS coils and under the control of PCS will be executed by IO, with the support of the DA. Although the integrated commissioning itself is not within the scope of this TA, the provisions of section 15.1.1 apply.

16 Packing, Delivery and Preservation Requirements

The DA is responsible for planning, assembly and installing the components at ITER worksite and management of administrative procedures (customs, export control…), with the support from IO.

Before each delivery, the DRR procedure [AD26] shall be followed to check the readiness of the delivery and approve the delivery activities.

16.1 Transport and Delivery

The Items shall be delivered to the ITER Site by the dates as reflected in the Detailed Working Schedule (DWS) at time of TA signature. The Items shall be delivered only upon completion of the Delivery Readiness Review in accordance with the "Working Instruction for the Delivery Readiness Review (DRR) (X3NEGB)" [AD26]. Transportation of the Items shall be carried out by the DA in accordance with the "Procedure for Transportation of Components to ITER Site (RY5C6Q)" [AD32].

The DA shall be responsible for delivering the Items to the ITER Site:

> ITER Organization
> Route de Vinon sur Verdon
> 13067 St Paul lez Durance
> France

and is encouraged to take an appropriate insurance policy coverage against risk of loss or damage to the Items during the transport.

The DA shall use the Global Transportation, Logistics and Insurance Services Framework Contract in accordance with the MoU "Global Transportation MOU EU DA (6KWXUQ)".

The DA shall be responsible for clearly labelling the Items and providing official documentation stating that export is performed on behalf of the IO pursuant to Articles 5 and 6 of the Agreement on the Privileges and Immunities of the ITER Organization (2ET9RX) (hereinafter referred to as the "P&I Agreement") and for its official activities.

The DA shall ensure that the Items to be delivered are safely and properly packaged conditioned and handled during transport and fulfil the specific requirements detailed in the Technical Specification.

The DA shall ensure that any export licence or authorization is obtained, if applicable, and shall carry out all applicable customs formalities necessary for the export of the Items in compliance with Articles 5 and 6 of the P & I Agreement and for their transit through any country.

The IO shall ensure that any import licence or authorization is obtained and shall carry out all applicable customs formalities necessary for the import of the Items in compliance with Articles 5 and 6 of the P & I Agreement.

Should the IO make a duly justified request to postpone the delivery of the whole or part of the Items at least 60 (sixty) calendar days prior to the stipulated date of delivery, the DA shall be

responsible for providing storage, protection and maintenance for the Items free of charge, for a period up to 60 (sixty) calendar days from the stipulated date of dispatch from factory.

The IO shall provide the DA direction on future storage, protection or maintenance requirements no later than the 40th calendar day of the free-of-charge period of 60 (sixty) calendar days. If the period exceeds 60 (sixty) calendar days, the DA shall continue to provide storage, protection and maintenance. Actual duly documented and justified costs incurred by the DA during the period of time in excess of the aforementioned 60 (sixty) calendar days shall be reimbursed by the IO. Should the DA make a duly justified request to speed up the delivery of the whole or part of the Items; the DA and the IO will assess any consequences of this action and an agreement will be sought related to any consequent storage costs.

16.2 Packaging and preservation

All associated components shall be packaged in accordance with ITER specific packaging and preservation specifications to ensure protection against mechanical damage, environmental degradation (including humidity, temperature variations, and UV exposure), and electrostatic discharge (ESD).

Packaging can be segregated to two types:

- Type 1: packaging for the equipment that requires protection against shock, vibration, physical damage, water vapor, condensation, and weather.
- Type 2: packaging providing protection against physical and mechanical damage.

Cleanliness requirements include inspection and removal of dust and contamination before packaging.

16.3 Labelling and tagging

Packaging materials shall be clearly labelled with:

- The System's model number, serial number, and batch number.
- Handling instructions, including orientation and weight limitations.
- Environmental storage requirements (temperature, humidity).
- Hazardous materials warnings (if applicable).

16.4 Documentation Required

- Two copies of the Packing List, one inside and one outside the crate.
- One copy of the Quality Certification (Certificate of Conformance-CoC) inside the crate.
- One copy of MIP (inside the crate).

Numbered seals are used for delivery documentation to avoid acceptance if seals are open or numbers do not match.

17 Assembly and Installation Requirements

The DA shall be responsible for the assembly and installation of all VS3-PS systems, subsystems and components within their scope, as well as for the realization of all associated interfaces as defined in sections 9 and 10 of this technical specification.

Before the installation, a Construction Readiness Review (CRR) shall be organized to check the readiness of the documentation for installation (drawings and procedures) and to approve the start of installation activities.

17.1 Installation design

The DA shall minimise the installation efforts needed in B13 in order to comply with the defined installation schedule, by designing the system such that the majority of components pre-assembled, pre-tested and pre-wired at their factory, and in accordance with the modular design requirements specified in section 8.5.

During the design stage, the DA shall perform the installation design to identify the on-site installation activities, the required workflow, and their respective durations.

The installation design shall be submitted for review and acceptance by IO as part of the design review gate, and in all cases prior to the commencement of the manufacturing stage.

17.2 Site installation

For the installation activities within the scope of this Task Agreement, section 13 of the GMS [AD2] and section 13 of the GM3S [AD1] shall apply in full.

During Assembly & Installation activities, the DA shall attend all meetings related to buildings coordination and co-activity management.

During Assembly & Installation activities, the DA is responsible for Permit-To-Work Management, as defined in the ITER Site Permit to Work Procedure [AD67].

Since most of the works on the ITER site will be performed in Building 13, requiring a high level of cleanliness, the following requirement applies.

Prior to commencing installation activities, the DA shall submit its cleanliness strategy in accordance with Cleanliness Strategy [AD68], demonstrating that all applicable requirements have been considered and will be fulfilled.

The successful Commissioning Certificate Readiness (CCR) review indicates the installation stage is completed.

TASK AGREEMENT EXECUTION REQUIREMENTS

18 Handover & Post-Installation Services

18.1 Training

Before the completion of the Task Agreement, the DA shall train the IO staff members to the following tasks, but not limited to:

a) Operation of the VS3-PS system, including the configuration, control of the system
b) Maintenance of the VS3-PS system, including preventive and curative maintenance, firmware update (if required)
c) Dismantling of the VS3-PS system (temporarily or permanently).

The documents/files used for the training shall be provided to the IO.

19 IO Documents and IO Free Issue Items

19.1 IO Documents: technical input documentation

Under this scope of work, IO will deliver the following documents by the stated date:

Table 19-1: Technical input documentation

Ref	Title	Doc ID	Expected date
1	All IDM reference documents		*Upon request*
2	3D context models for Building 13		*Upon request*

19.2 Free issue items

Under this scope of work, IO will deliver the following equipment/parts by the stated date:

Table 19-2: Free issue items

Ref	Equipment / Part Description	Part No.	Expected date
1	Mini-CODAC		*Upon request before FAT*
2	Mini-CIS		*Upon request before FAT*

20 Deliverables and Milestone Schedule

20.1 Schedule for Milestones

The schedule for the milestones of the Task Agreement is specified in Table 20-1.

Table 20-1: VS3-PS TA Milestone Schedule

Milestone	Deliverables	Acceptance criteria	Date [1)]
T0	TA Signature Date		01/12/2026
KOM	TA domestic arrangement documentation package submission	Documents accepted by IO TA RO	31/01/2027
Design			
PDR	Preliminary Design Review completed	PDR deliverables and close-out report accepted by IO TA RO	31/12/2027
FDR	Final Design Review completed	FDR deliverables and close-out report accepted by IO TA RO	30/11/2028
MRR	Manufacturing Readiness Review completed	MRR deliverables accepted by IO TA RO	30/04/2029
Manufacturing & Factory Acceptance Testing			
Manufacturing	Manufacturing of components completed	Manufacturing of components and deliverables accepted by IO TA RO	30/04/2030
FAT	Factory Acceptance Tests completed	All FAT reports accepted by IO TA RO	31/07/2030
DRR	Delivery Readiness Review completed	DRR deliverables accepted by IO TA RO	30/09/2030
Delivery, Installation & Site Acceptance Testing			
CRR	Construction Readiness Review completed	CRR deliverables accepted by IO TA RO	30/06/2031
CCR	Commissioning Certificate Readiness completed	CCR deliverables accepted by IO TA RO	30/04/2032
SAT	Site Acceptance Tests completed	All SAT reports accepted by IO TA RO	30/09/2032
TA Completion Review	TA Completion Review with the final deliverables.	Final deliverables accepted by IO TA RO and Final Acceptance Certificates issued to DA.	31/12/2032

Note 1: based on TA Signature Date of 01/12/2026

20.2 List of deliverable documentation

The DA shall provide IO with the material, documents and data required in the application of this technical specification, the Expected content of System Design deliverables [AD24], the Template for SDR Input Data Package [RD38] and any other requirement derived from the application of the Task Agreement.

A deliverable document list, consistent with the Expected content of System Design deliverables [AD24], will be provided by IO to the DA, which it may adopt as minimum list reference.

The final list is to be prepared by the DA and accepted by the IO at each Review Gate and each document approved by the IO before the respective TA gate, as defined in chapter 13.

21 Quality Requirements

Quality Requirements shall be in accordance with the Quality Requirements for IO Performers [AD7]. For this purpose, the DA and subcontractors carrying out contracts placed under this Task Agreement shall be in compliance with the QA requirements under the relevant ITER QA classification Quality Classification Determination [AD35] and shall have an IO approved QA Program or an ISO 9001 accredited quality system, complemented with the above mentioned requirements.

Prior to commencement of the works, the DA shall submit a Quality Plan for IO approval in accordance with Quality Requirements for IO Performers [AD7]. The Quality Plan shall describe the organisation for tasks; roles and responsibilities of workers involved in; any anticipated subcontractors; and give details of who are the independent checkers of the activities. The Quality Plan shall be sent to the IO-RO who will upload it in IDM with the relevant IO QA-RO as a reviewer. After considering any comments in IDM, the IO-RO will inform his approval/disapproval to the DA-RO. Quality Plans shall be produced by the DA's Suppliers and Subcontractors and submitted to the IO for acceptance, unless otherwise agreed between the Parties, to describe how they will implement the ITER Procurement Quality Requirements.

Manufacturing and Inspection Plans (MIP) are used to monitor Quality Control and acceptance tests and must be produced by each Supplier and Subcontractor and submitted to the IO for acceptance and mark-up of any IO interventions, unless otherwise agreed between the Parties. It should be noted that interventions additional to those required in the Technical Specification may be included on the MIP by IO if justified.

When a deviation to an IO specified requirement is anticipated, the DA shall discuss it with the IO-RO as appropriate for that ITER work activity. If the proposed deviation is considered beneficial, in accordance with the Procedure for the Management of Deviation Request [AD8], a Deviation Request shall be submitted to IO for a decision using the Deviation Request Template [RD37].

When a non-conformity is identified, the DA shall inform the IO-RO immediately or as soon as practically possible, of the nature of the non-conformity, taking into account requirements and process described in the Procedure for Management of Nonconformities [AD9]. If needed, immediate actions shall be applied, to segregate a nonconforming item or work in order to ensure safety. After confirmation of agreement on categorization, the DA shall issue a Non-Conformance Report using the NCR Database.

Documentation developed as the result of the work shall be retained by the DA or a subcontractor for a minimum of five (5) years and then may be discarded at the direction of the IO.

IO will monitor implementation of the DA's Quality Plan. Where necessary, IO will assess the adequacy and effectiveness of the quality management system specified in the Quality Plan through inspections or audit. Where condition adverse to quality is identified, the DA shall eliminate discovered findings.

The use of computer software to perform a safety basis task activity such as analysis and/or modelling, etc. shall be reviewed and approved by the IO prior to its use in accordance with

Working Instruction for the Qualification of ITER safety codes [AD36]. The Software Qualification Policy [AD42] shall be taken into consideration where applicable to ensure quality and integrity of software prior to application.

22 Special Management Requirements

22.1 Long-Lead Items

Long-lead items are defined as components or raw materials whose lead time – including manufacturing and delivery – does not permit meeting the contractual milestone dates when activity phases and associated gate reviews are executed in accordance with the applicable procedures

In accordance with the applicable procedures, the DA is not permitted to procure components or raw materials prior to completion of the MRR. However, IO may grant deviations allowing the procurement of long-lead items before the completion of the relevant gate reviews (PDR, FDR, MRR, etc.).

At the earliest stage of the Task Agreement, the DA shall identify and substantiate the long-lead items. The risk or opportunity associated with procuring long-lead items prior to completion of the relevant gate reviews shall be recorded in the Risk and Opportunity Register and monitored accordingly.

For each long-lead item, the Contractor shall substantiate that its lead time is incompatible with the Task Agreement schedule and that it complies with all applicable VS3-PS system requirements, Task Agreement requirements, and the corresponding future gate reviews.

Procurement of long-lead items shall not commence without the IO's prior acceptance.

22.2 Risk Management

The DA shall, within 90 (ninety) calendar days of the entry into force of the TA, draw up and submit to the IO, for information, a plan for managing risks associated with implementing the TA (hereinafter referred to as the "TA Risk Plan").

The TA Risk Plan will be consistent with the "Risk and Opportunity Management Procedure (22F4LE)" [AD56] and implemented through the DA Project Risk Management Process.

The DA shall process risks which may impinge on the successful execution of the TA directly in the Project Risk Register, in accordance with the "Risk and Opportunity Management Procedure (22F4LE)" [AD56].

The DA shall implement RAMI engineering standards for the execution of the TA according to "ITER RAMI Analysis Program (28WBXD)" [AD10].

22.3 Environment, Safety and Health and Security

The DA shall ensure that its personnel, Contractors and Subcontractors observe all applicable environment, safety and health and security provisions for work on the ITER Site in Cadarache, as well as specific requirements set out in the Technical Specification.

Any activity by DA personnel or its Contractors and Subcontractors at the ITER Site shall be subject to the "Internal Regulations (27WDZW)" [AD60] and "Contractor Safety Management Procedure (Q2GBJF)" [AD58].

Any activity by DA personnel or its Contractors and Subcontractors on the ITER Construction Site shall be subject to the "Health Protection and Safety General Coordination Plan - ITER Construction Site - volume 0- General Safety Rules (2NUEYG)" [AD59] and resulting procedures. Any additional applicable provisions regarding environment, safety and health and Security, as well as Project Control and Site Coordination, shall be communicated by the IO to the DA at least 30 (thirty) calendar days in advance of the activities to be performed at the ITER Site.

For all entities working on Site, the following documents shall apply for work on the ITER Construction Site:

- "Environmental requirements (97WRFP)" [AD61],
- "ITER Policy on Safety, Security and Environment Protection Management (43UJN7)" [AD57],
- "Contractor Safety Management Procedure (Q2GBJF)" [AD58],
- "ITER Site access Procedure (S3893D)" [AD62],
- "Procedure for Occupational Health and Safety Hazard Identification and Assessment (AJLQRF)" [AD64],
- "Vehicle Access and Traffic Circulation and Parking on the ITER Site (N3MG3V)" [AD65].
- "MQP L2 Physical Security Protection Management Procedure (TZYDJH)" [AD66].

The DA personnel and its Contractors and Subcontractors on the ITER Construction Site shall be subject to the "General Management Specification for Executing Entities at the ITER Site (YX55YY)" [AD2], which collects in a consistent manner existing requirements already applicable, as well as requirements in the field of Project Control and Site Coordination.

22.4 Licensing Requirements (for PED)

For Items under PED the following applies:

Certain Items that are the subject of this TA are subject to the requirements of the Pressure Equipment Directive (PED) [CS31], implemented in France by the Articles L557 and R557 of the French Environment Code. The design and manufacture of these Items must conform with the Articles L557 and R557 of the French Environment Code. For certain categories of equipment, the conformity assessment must be performed by a Notified Body[1].

Pursuant to Article 14 of the ITER Agreement, the IO and DA shall apply all applicable rules

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1   Notified Body is a company that has been nominated by a European Union Member State and notified to the European Commission for pressure equipment conformity assessment.

and regulations resulting from French Laws and Regulations with respect to Licensing "Nuclear Regulatory Framework for INB ITER (2WBB8P)".

If and when the IO establishes rules and regulations after signature of this TA in order to comply with the French regulatory requirements in force at the time of signature, the DA shall ensure to conform to those.

APPENDICES

23 APPENDICES

A   Existing anchors in B13

There are three types of existing anchoring systems designed for the fixation of the SSAT tools, which may be reused by DA for the fixation of VS3-PS components. The three types are identified as A, A1 and A2 and described below.
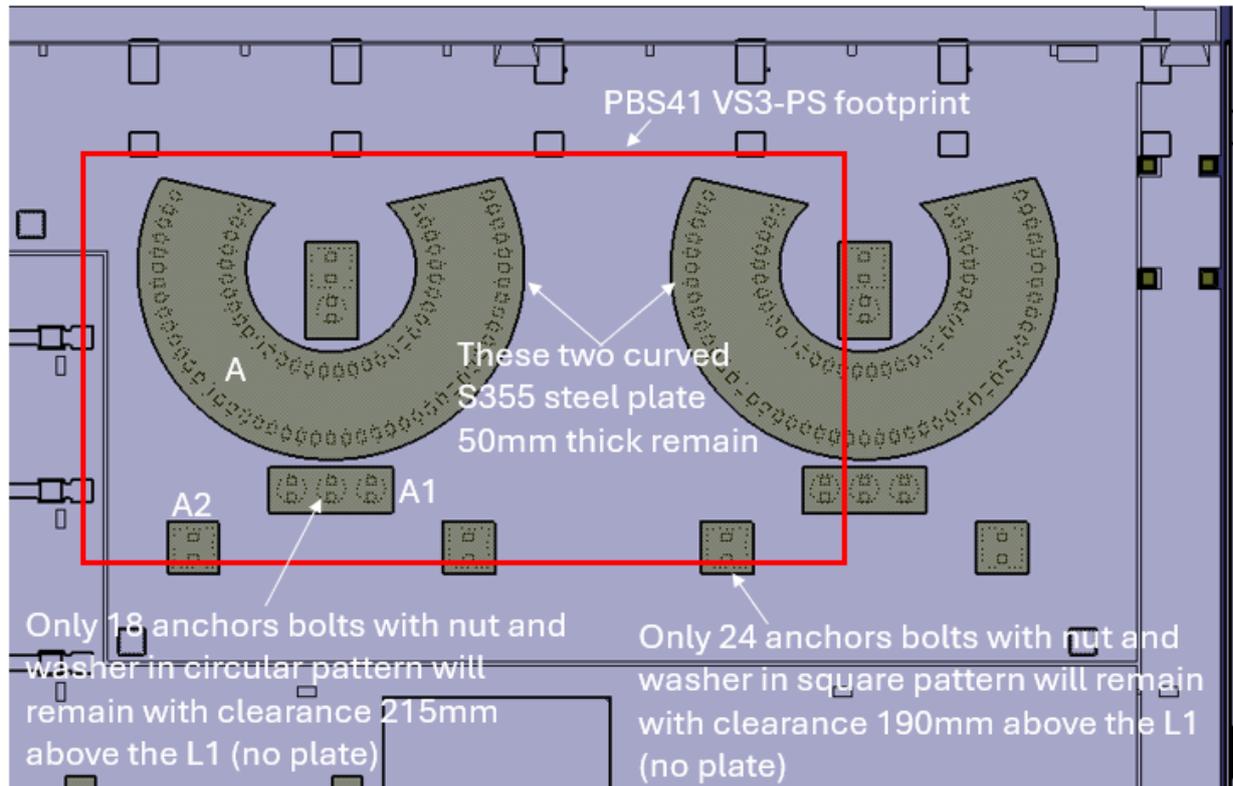
Figure 23-1: locations of existing anchors in the B13 slab, with the reserved VS3-PS floor area in red

A.1   Existing anchor Type A

Anchors of type A are originally used for the fixation of the rails of the SSATs.

The remaining anchoring components after the removal of the SSAT tools agreed with PBS22 in reference [AD78] are shown (in green) in Figure 23-2.

The remaining components are the seventeen 50mm thick rail base plates presented in drawings THA100000000A_76G001 to 18 and the anchor bolts shown in Figure 23-2.

The existing bolts M30 with their nuts as well as all the threaded holes in the plates shall be protected by all necessary means to avoid impact or any kind of damage.

All accidental hitting of the rail base plates or the existing M30 bolts during the handling of components shall be avoided.

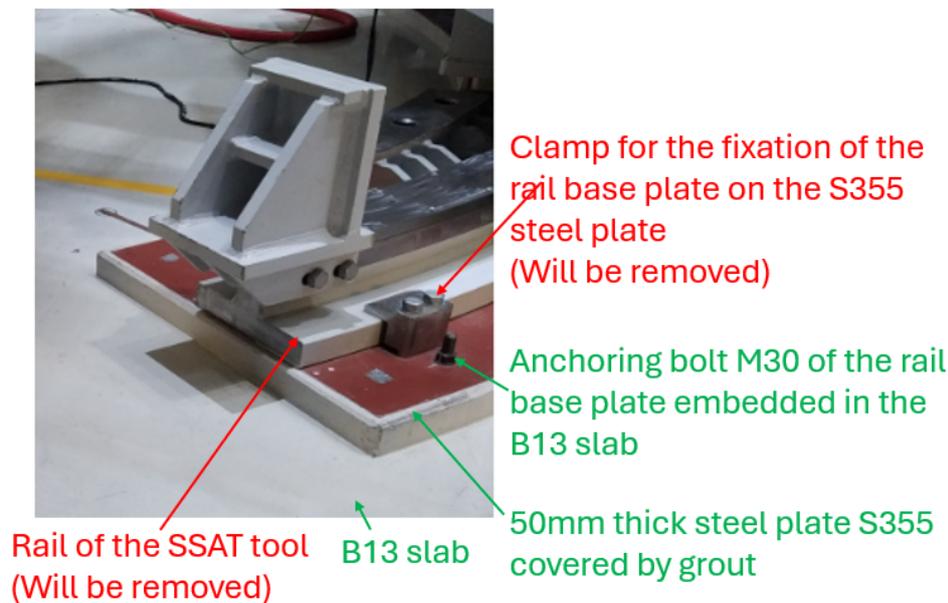The flatness of the rail base plates shall not be altered.

Clamp for the fixation of the rail base plate on the S355 steel plate (Will be removed)

Anchoring bolt M30 of the rail base plate embedded in the B13 slab

50mm thick steel plate S355 covered by grout

Rail of the SSAT tool (Will be removed)

B13 slab

Figure 23-2: existing Type A anchors in the B13 slab

A.1.1   Reusing Type A anchors

Should these anchor points be reused for VS3-PS anchoring purposes, the capacity of all existing threaded holes and the capacity of the plates shall be determined based on [RD55], and the limits of these existing components that shall not be exceeded shall be clearly defined. Then the torque adapted to the capacity of the threaded holes shall be set accordingly on the tightening tool.

Suitable tightening tools shall be used while tightening or untightening screws in any of the existing threaded holes in the plates.

A.2   Existing anchor Type A1

The anchor type A1 is composed of 18 anchors M42 in a circular pattern of Φ1300 used for the fixation of columns in front of the SSATs. In the middle of the area, there are two recesses (shear keys) in the concrete as shown in Figure 23-3. The dimension of each recess is 390mm x 360mm x 325mm.

The remaining anchoring components after the removal agreed with PBS 22 in [AD78] are the 18 anchor bolts according to drawings in [RD56] and [RD57].

All the necessary measures shall be taken to avoid damage to the existing anchors during installation. All accidental hitting of the existing M42 bolts during the handling of components is to be avoided.

Ingress of debris into the steel sleeves of the anchors shall be avoided in case the installed protections are removed.

In case some of the existing M42 bolts are not used, they shall be protected by all means to avoid impact or any kind of damage, insofar the appropriate protections are not already present.
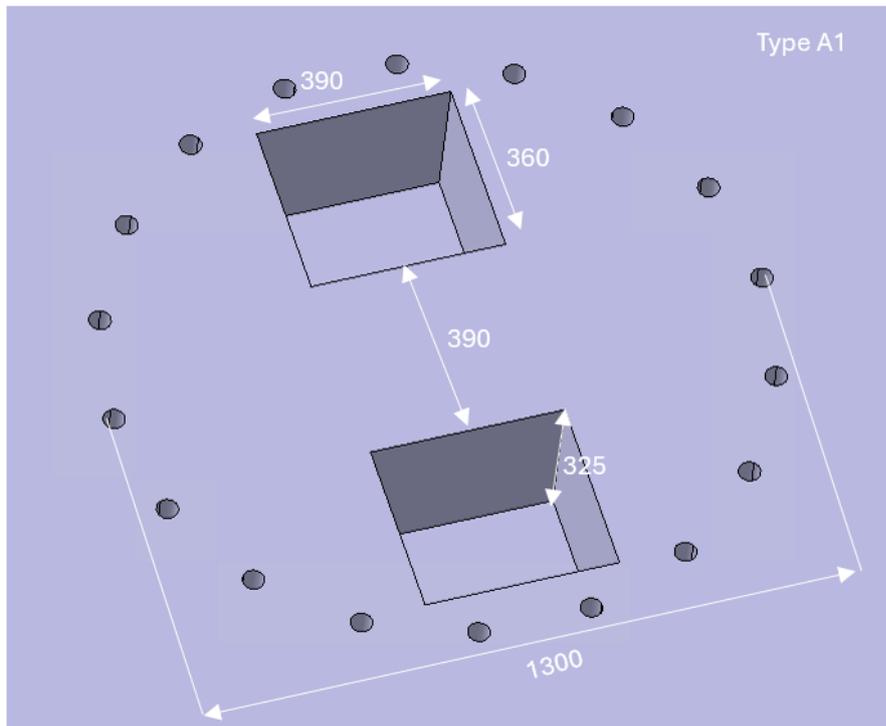
Figure 23-3: hole pattern and shear keys of anchor Type A1

A.2.1   *Reusing Type A1 anchors*

Should these anchor points be reused for VS3-PS anchoring purposes, then the capacity of all the remaining eighteen M42 anchor bolts shall be determined using [RD50], and the limits in terms of mechanical resistance shall not be exceeded.

The DA may use a 50mm thick S355 steel plate (or higher) with the 385mm height HEM360 beams welded on the plate to fit into the existing recesses. The VS3-PS components can subsequently be welded on the anchor plate. The HEM360 beam increases the shear resistance of the anchor and limits the bending of the plate. The anchor plate is to be anchored using the existing bolts.

Suitable tightening tools shall be used while tightening or untightening any of the existing bolts.

Then the torque adapted to the capacity of the anchor bolts shall be set accordingly on the tightening tool.

In addition, the following requirements/limits apply:

-   the bolts shall be maintained concentrically with the holes within a tolerance of ±10mm
-   the center of the holes of bolts in the plate shall be 150mm from the edge of the plate
-   the plate shall be equipped with two 30mm diameter through holes located at 150mm from the center of the plate for grouting purposes

In order to avoid the cracking of the edges of the concrete, grout shall be filled back in the space between the plate and the concrete. An example is provided in Figure 23-5.
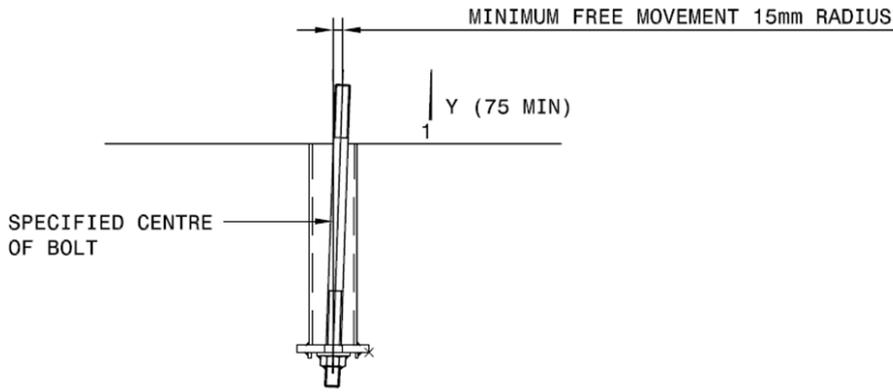
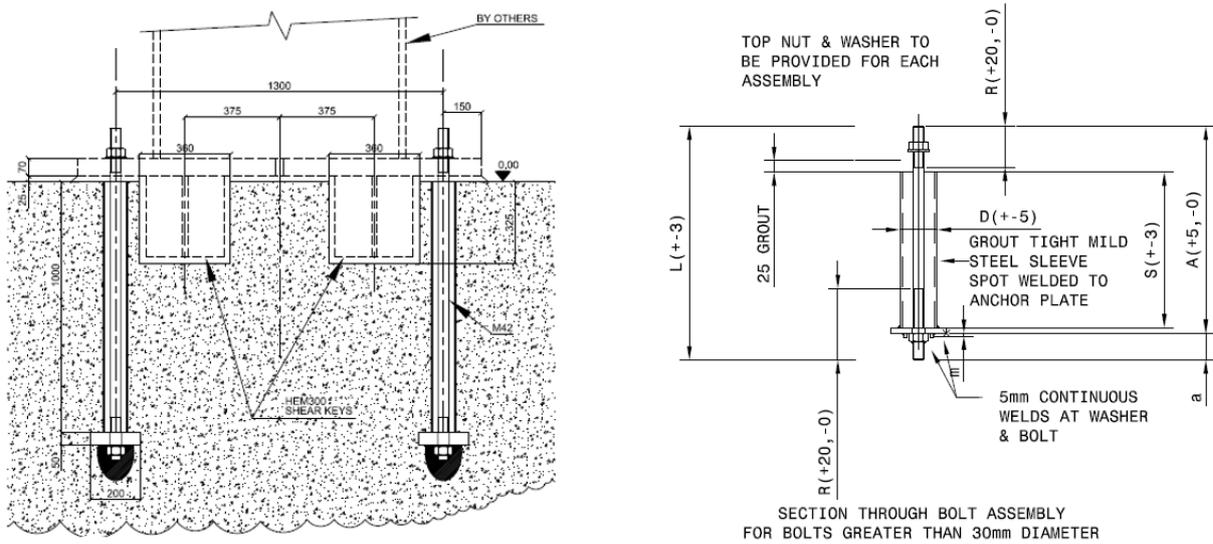Figure 23-4: free movement of one Type A1 anchor

Figure 23-5: Type A1 anchor with its anchor plate

A.3 Existing anchor Type A2

The anchor Type A2 is composed of 1800x1800 square pattern of 24 anchors M24 used for the fixation of columns. In the middle of the area, there is a recess in the concrete as shown in Figure 12. The dimension of the recess is 445mm x 358mm x 385mm.

The remaining anchoring components after the removal agreed with PBS 22 in [AD78] are the 24 anchor bolts according to drawings in [RD56] and [RD57].

All the necessary measures shall be taken to avoid damage to the existing anchors during installation. All accidental hitting of the existing M24 bolts during the handling of components is to be avoided.

Ingress of debris into the steel sleeves of the anchors shall be avoided in case the installed protections are removed.

In case some of the existing M24 bolts are not used, they shall be protected by all means to avoid impact or any kind of damage, insofar the appropriate protections are not already present.
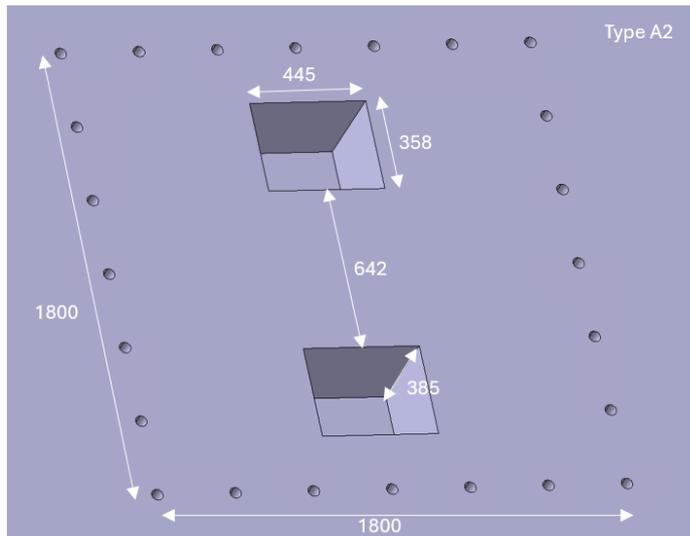
Figure 23-6: hole pattern and shear keys of anchor Type A2

A.3.1   Reusing Type A2 anchors

Should these anchor points be reused for VS3-PS anchoring purposes, then the capacity of all the remaining twenty-four M24 anchor bolts shall be determined using [RD50], and the limits in terms of mechanical resistance shall not be exceeded.

The DA may use a 50mm thick S355 steel plate (or higher) with the 385mm height HEM360 beams welded on the plate to fit into the existing recesses. The VS3-PS components can subsequently be welded on the anchor plate. The HEM360 beam increases the shear resistance of the anchor and limits the bending of the plate. The anchor plate is to be anchored using the existing bolts.

Suitable tightening tools shall be used while tightening or untightening any of the existing bolts.

Then the torque adapted to the capacity of the anchor bolts shall be set accordingly on the tightening tool.

In addition, the following requirements/limits apply:

-   the bolts shall be maintained concentrically with the holes within a tolerance of ±10mm
-   the center of the holes of bolts in the plate shall be 150mm from the edge of the plate
-   the plate shall be equipped with two 30mm diameter through holes located at 150mm from the center of the plate for grouting purposes

In order to avoid the cracking of the edges of the concrete, grout shall be filled back in the space between the plate and the concrete. An example is provided in Figure 23-5.
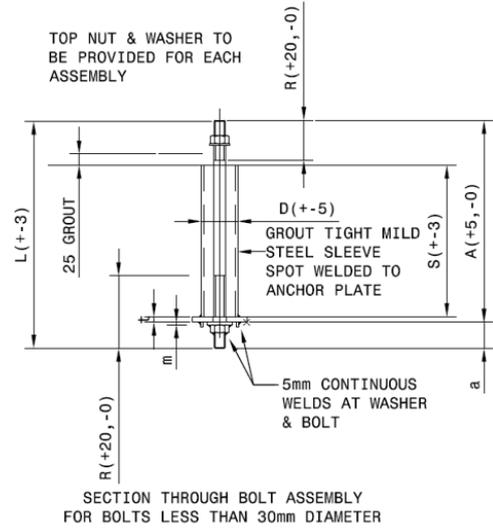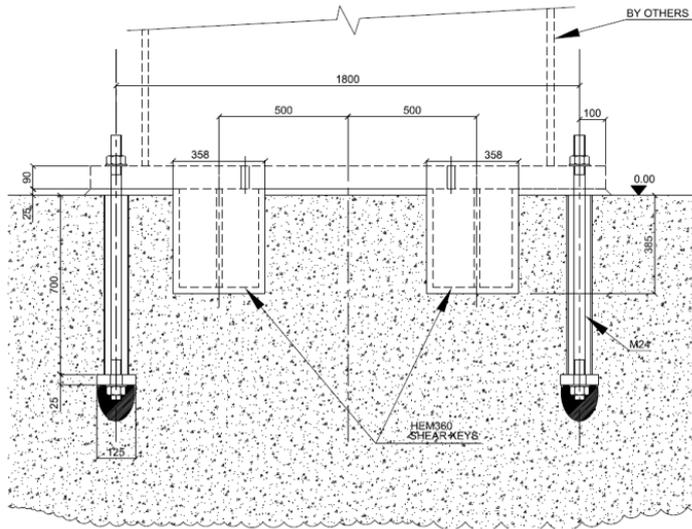
Figure 23-7: Type A2 anchor with its anchor plate

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